UNIT-5- MEMORY DEVICES AND DIGITAL INTEGRATED CIRCUITS

MEMORY AND PROGRAMMABLE LOGIC.

MEMORIES:

INTRODUCTION

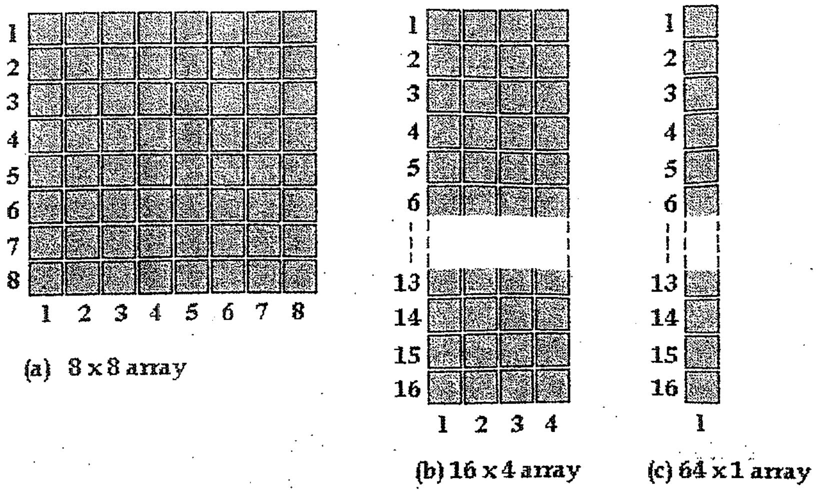
A memory unit is a collection of storage cells with associated circuits needed to transfer information in and out of the device. The binary information is transferred for storage and from which information is available when needed for processing. When data processing takes place, information from the memory is transferred to selected registers in the processing unit. Intermediate and final results obtained in the processing unit are transferred back to be stored in memory.

* Units of Binary Data: Bits, Bytes, Nibbles and Words

As a rule, memories store data in units that have from one to eight bits. The smallest unit of binary data is the bit. In many applications, data are handled in an 8-bit unit called a **byte** or in multiples of 8-bit units. The byte can be split into two 4-bit units that are called **nibbles**. A complete unit of information is called a **word** and generally consists of one or more bytes. Some memories store data in 9-bit groups; a 9-bit group consists of a byte plus a parity bit.

* Basic Semiconductor Memory Array

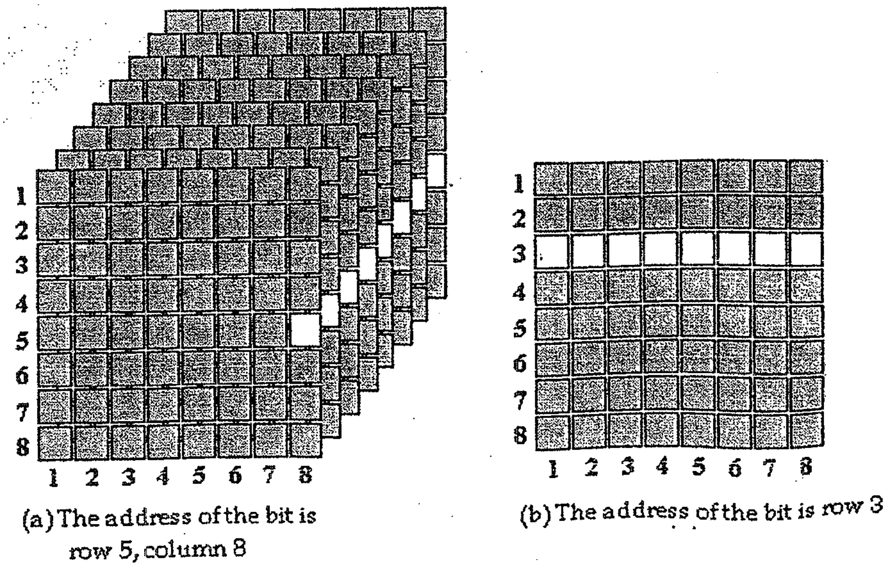
Each storage element in a memory can retain either a 1 or a 0 and is called a cell. Memories are made up of arrays of cells, as illustrated in Figure below using 64 cells as an example. Each block in the memory array represents one storage cell, and its location can be identified by specifying a row and a column.



A 64-cell memory array organized in three different ways

Memory Address and Capacity

The *location* of a unit of data in a memory array is called its address. For example, in Figure (a), the address of a bit in the 3-dimensional array is specified by the row and column. In Figure (b), the address of a byte is specified only by the row in the 2-dimensional array. So, as you can see, the address depends on how the memory is organized into units of data. Personal computers have random-access memories organized in bytes. This means that the smallest group of bits that can be addressed is eight.



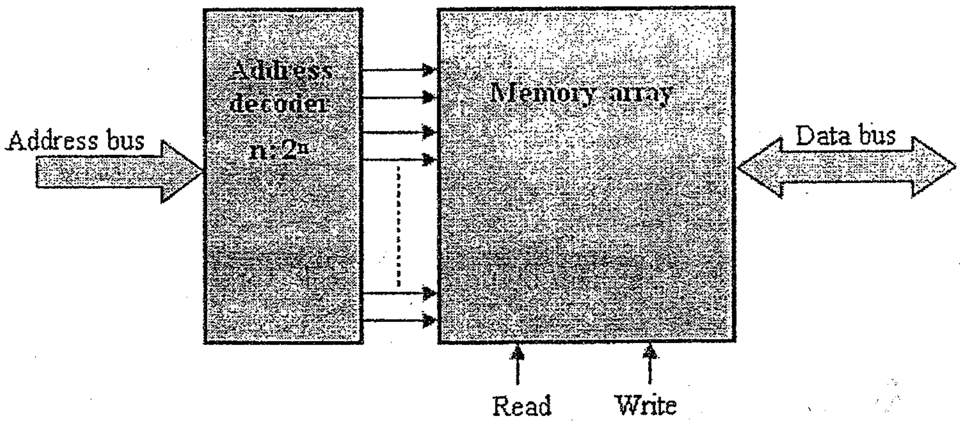
Examples of memory address

The **capacity** of a memory is the total number of data units that can be stored. For example, in the bit-organized memory array in Figure (a), the capacity is 64 bits. In the byte-organized memory array in Figure (b), the capacity is 8 bytes, which is also 64 bits. Computer memories typically have 256 MB (megabyte) or more of internal memory.

Basic Memory Operations

Since a memory stores binary data, data must be put into the memory and data must be copied from the memory when needed. The write operation puts data into a specified address in the memory, and the read operation copies data out of a specified address in the memory. The addressing operation, which is part of both the write and the read operations, selects the specified memory address.

Data units go into the memory during a write operation and come out of the memory during a read operation on a set of lines called the *data bus*. As indicated in Figure, the data bus is bidirectional, which means that data can go in either directional (into the memory or out of the memory).



Block diagram of memory operation

For a write or a read operation, an address is selected by placing a binary code representing the desired address on a set of lines called the address bus. The address code is decoded internally and the appropriate address is selected. The number of lines in the address bus depends on the capacity of the memory. For example, a 15-bit address code can select 32,768 locations (2^{15}) in the memory; a 16-bit address code can select 65,536 locations (2^{16}) in the memory and so on.

In personal computers a 32-bit address bus can select 4,294,967,296 locations (2^{32}), expressed as 4GB.

Write Operation

To store a byte of data in the memory, a code held in the address register is placed on the address bus. Once the address code is on the bus, the address decoder decodes the address and selects the specified location in the memory. The memory then gets a write command, and the data byte held in the data register is placed on the data bus and stored in the selected memory address, thus completing the write operation. When a new data byte is written into a memory address, the current data byte stored at that address is overwritten (replaced with a new data byte).

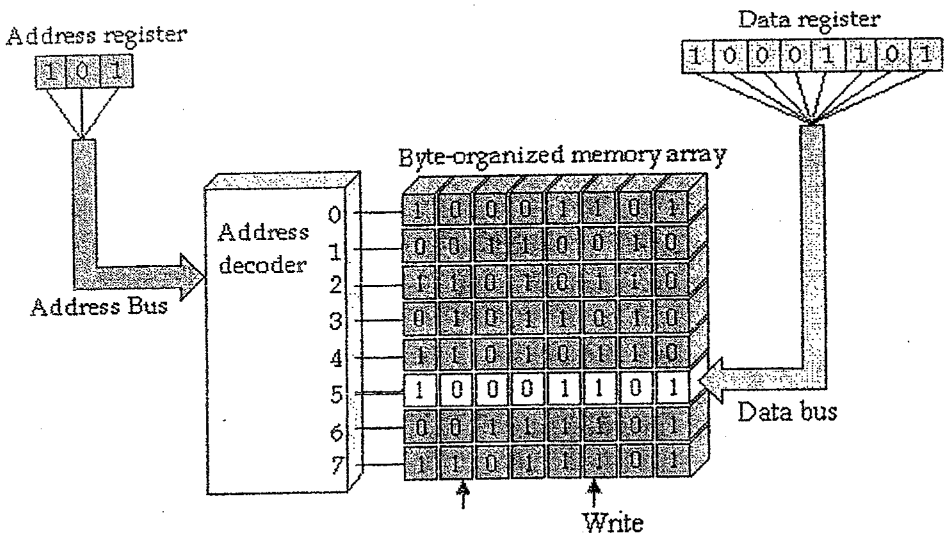


Illustration of the Write operation

Read Operation

A code held in the address register is placed on the address bus. Once the address code is on the bus, the address decoder decodes the address and selects the specified location in the memory. The memory then gets a read command, and a "copy" of the data byte that is stored in the selected memory address is placed on the data bus and loaded into the data register, thus completing the read operation. When a data byte is read from a memory address, it also remains stored at that address. This is called *nondestructive* read.

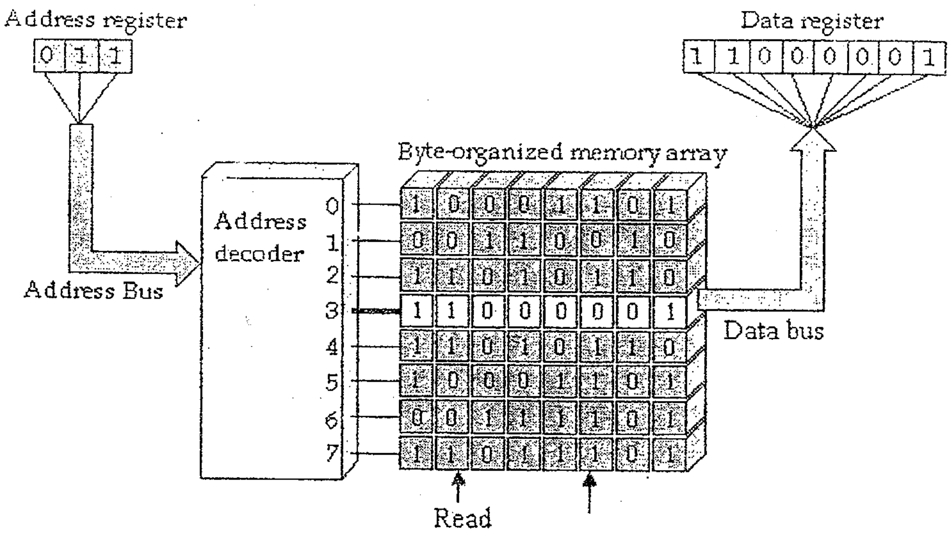


Illustration of the Read operation

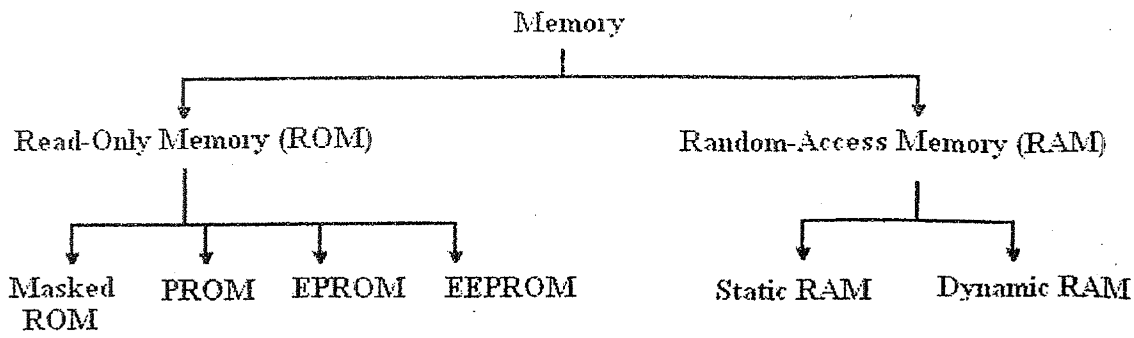
Classification of Memories

There are two types of memories that are used in digital systems:

- Random-Access Memory (RAM),
- Read-Only Memory (ROM).

1. **RAM** (random-access memory) is a type of memory in which all addresses are accessible in an equal amount of time and can be selected in any order for a read or write operation. All RAMs have both read and write capability. Because RAMs lose stored data when the power is turned off, they are ***volatile*** memories.

2. **ROM** (read-only memory) is a type of memory in which data are stored permanently or semi permanently. Data can be read from a ROM, but there is no write operation as in the RAM. The ROM, like the RAM, is a random-access memory but the term RAM traditionally means a random-access read/write memory. Because ROMs retain stored data even if power is turned off, they are ***nonvolatile*** memories.



Classification of memories

RANDOM-ACCESS MEMORIES (RAMS)

RAMs are read/write memories in which data can be written into or read from any selected address in any sequence. When a data unit is written into a given address in the RAM, the data unit previously stored at that address is replaced by the new data unit. When a data unit is read from a given address in the RAM, the data unit remains stored and is not erased by the read operation. This nondestructive read operation can be viewed as copying the content of an address while leaving the content intact.

A RAM is typically used for short-term data storage because it cannot retain stored data when power is turned off.

The two categories of RAM are the ***static* RAM** (SRAM) and the ***dynamic* RAM** (DRAM). Static RAMs generally use flip-flops as storage elements and can therefore store data indefinitely *as long as dc power is applied*. Dynamic RAMs use capacitors as storage elements and cannot retain data very long without the capacitors being recharged by a process called refreshing. Both SRAMs and DRAMs will lose stored data when dc power is removed and, therefore, are classified as *volatile memories*.

Data can be read much faster from SRAMs than from DRAMs. However, DRAMs can store much more data than SRAMs for a given physical size and cost because the DRAM cell is much simpler, and more cells can be crammed into a given chip area than in the SRAM.

I. Static RAM (SRAM)

Storage Cell:

All static RAMs are characterized by flip-flop memory cells. As long as dc power is applied to a static memory cell, it can retain a 1 or 0 state indefinitely. If power is removed, the stored data bit is lost.

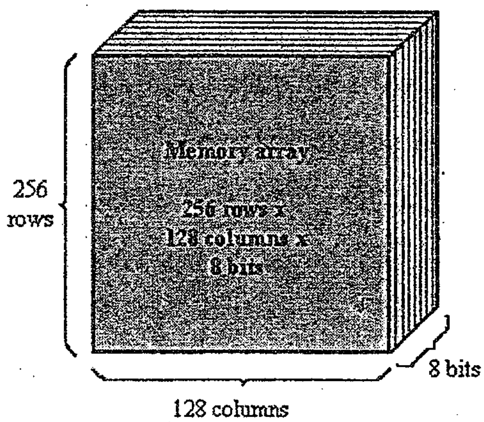
The cell is selected by an active level on the Select line and a data bit (1 or 0) is written into the cell by placing it on the Data in line. A data bit is read by taking it off the Data out line.

Basic SRAM Organisation:

Basic Static Memory Cell Array

The memory cells in a SRAM are organized in rows and columns. All the cells in a row share the same Row Select line. Each set of Data in and Data out lines go to each cell in a given column and are connected to a single data line that serves as both an input and output (Data I/O) through the data input and data output buffers.

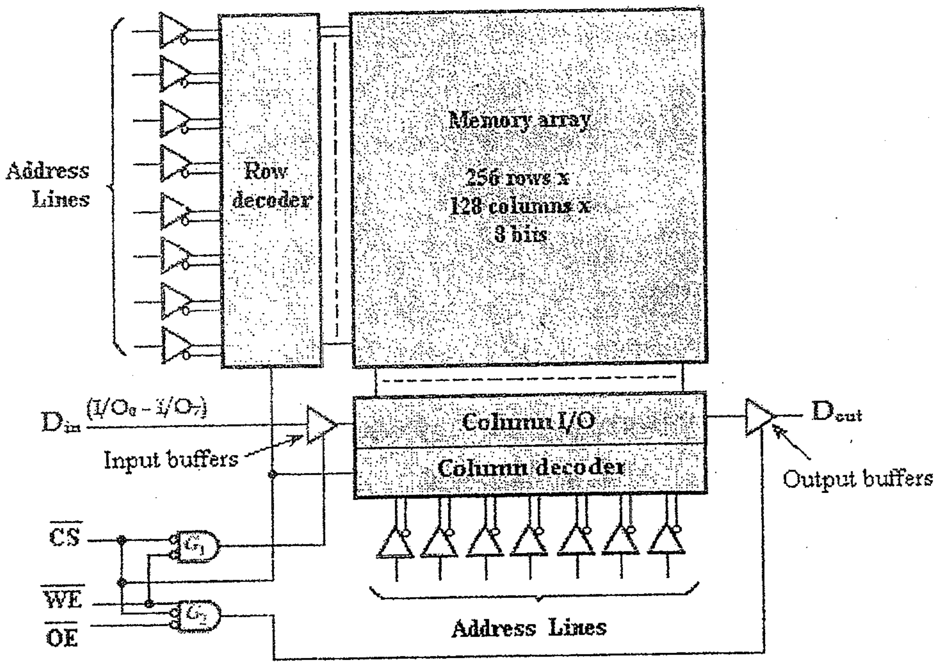
SRAM chips can be organized in single bits, nibbles (4 bits), bytes (8 bits), or multiple bytes (16, 24, 32 bits, etc.). The memory cell array is arranged in 256 rows and 128 columns, each with 8 bits as shown below. There are actually 2^{15} = 32,768 addresses and each address contains 8 bits. The capacity of this example memory is 32,768 bytes (typically expressed as 32 kbytes).



Memory array configuration

Operation:

The SRAM works as follows. First, the chip select, CS, must be LOW for the memory to operate. Eight of the fifteen address lines are decoded by the row decoder to select one of the 256 rows. Seven of the fifteen address lines are decoded by the column decoder to select one of the 128 8-bit columns.



Memory block diagram

Read:

In the READ mode, the write enable input, WE′ is HIGH and the output enable, OE′ is LOW. The input tristate buffers are disabled by gate G_1, and the column output tristate buffers are enabled by gate G_2. Therefore, the eight data bits from the selected address are routed through the column I/O to the data lines (I/O_1 through I/O_7), which are acting as data output lines.

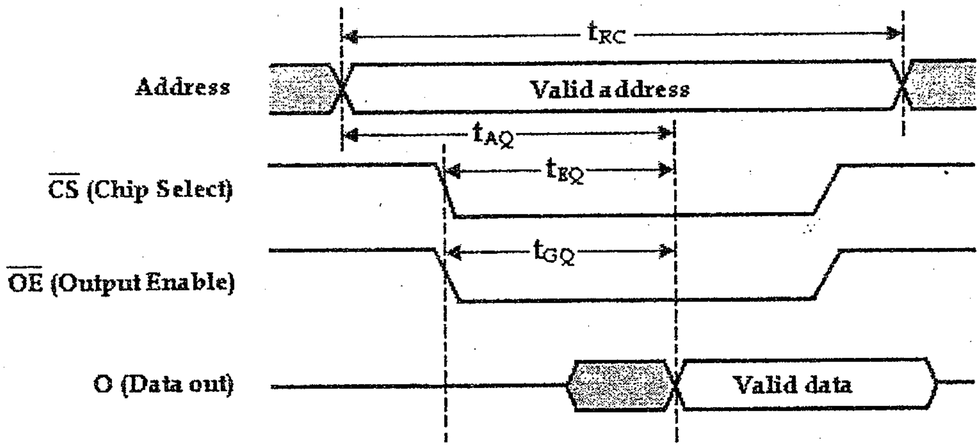
Write:

In the WRITE mode, WE′ is LOW and OE′ is HIGH. The input buffers are enabled by gate G_1, and the output buffers are disabled by gate G_2. Therefore the eight input data bits on the data lines are routed through the input data control and the column I/O to the selected address and stored.

Read and Write Cycles:

For the read cycle shown in part (a), a valid address code is applied to the address lines for a specified time interval called the *read cycle time*, t_{WC}. Next, the chip select (CS) and the output enable (DE) inputs go LOW. One time interval after the DE input goes LOW; a valid data byte from the selected address appears on the data lines. This time interval is called the ***output enable access time***, t_{GQ}. Two other access times for the read cycle are the ***address access time***, t_{AQ}, measured from the beginning of a valid address to the appearance of valid data on the data lines and the **chip enable access time**, t_{EQ}, measured from the HIGH-to-LOW transition of CS to the appearance of valid data on the data lines.

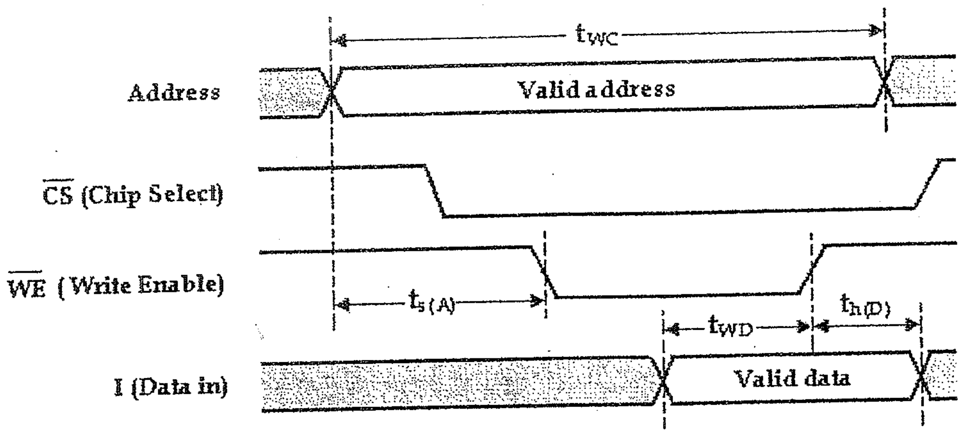
During each read cycle, one unit of data, a byte in this case is read from the memory.



(a) Read Cycle ($\overline{WE}$ HIGH)

For the write cycle shown in Figure (b), a valid address code is applied to the address lines for a specified time interval called the *write cycle time*, t_{WE} . Next, the chip select (CS) and the write enable (WE) in puts go LOW. The required time interval from the beginning of a valid address until the WE input goes LOW is called the ***address setup time***, $t_{s(A)}$. The time that the WE input must be LOW is the write pulse width. The time that the input WE must remain LOW after valid data are applied to the data inputs is designated t_{WD}; the time that the valid input data must remain on the data lines after the WE input goes HIGH is the data hold time, $t_{h(D)}$.

During each write cycle, one unit of data is written into the memory.



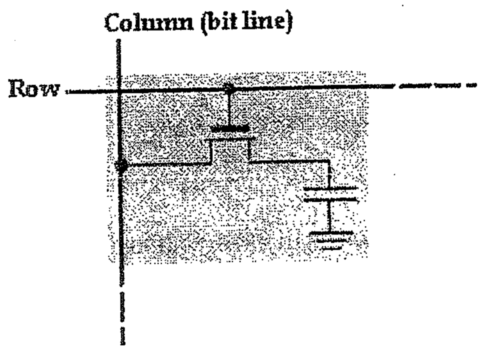
(b) Write cycle (WE LOW)

Dynamic RAM (DRAM)

Dynamic RAM Cell:

Dynamic memory cells store a data bit in the form of electric charges on capacitors. The basic storage device in DRAM is not a flip-flop but a simple MOSFET and a capacitor.

The advantage of this type of cell is that it is very simple, thus allowing very large memory arrays to be constructed on a chip at a lower cost per bit. The disadvantage is that the storage capacitor cannot hold its charge over an extended period of time and will lose the stored data bit unless its charge is refreshed periodically. To refresh requires additional memory circuitry and complicates the operation of the DRAM.



DRAM memory cell

In DRAM memory cell, a bit of data is stored as charge on storage capacitor, where the presence or absence of charge determines the value of the stored bit 1 or 0.

The DRAM cell includes a single MOS transistor (MOSFET) and a capacitor. When column line and row line go high, the MOSFET conducts and charges the capacitor. When the column and row lines go low, the MOSFET opens and the capacitor retains its charge. In this way it stores 1 bit.

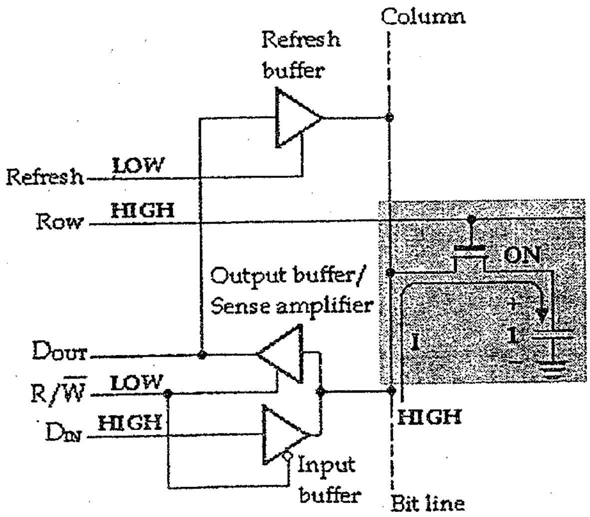
Operation:

The DRAM cell consists of 3 tri-state buffers: Input buffer, Output buffer and refresh buffer. Input and output buffers are enabled and disabled by controlling R/W′ line. When R/W′= 0, input buffer is enabled and output buffer is disabled. When R/W′= 1, input buffer is disabled and output buffer is enabled.

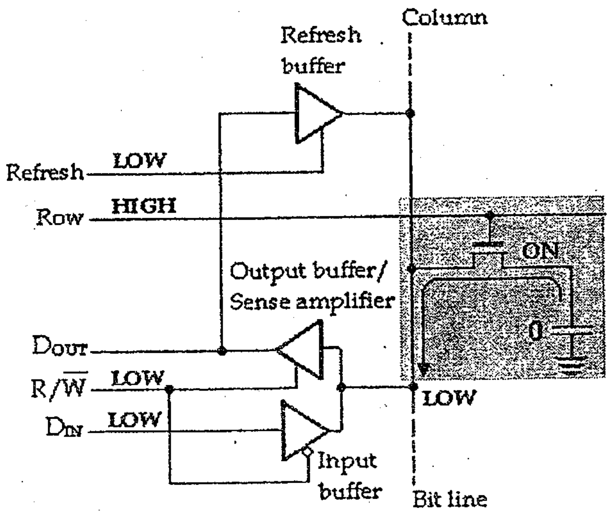
(i) **Write:**

To enable write operation R/W′ line is made low, which enables input buffer and disables output buffer. To write a 1 into the cell, the D_{IN} line is high and MOSFET is turned ON by a high on the row line. This allows the capacitor to charge to a positive voltage. When 0 is to be stored, a low is applied to the D_{IN} line. The capacitor remains unchanged or if it is storing a 1, it discharges.

When the row line is made low, the transistor turns OFF and disconnects the capacitor from the data line, thus storing the charge (1 or 0) on the capacitor.



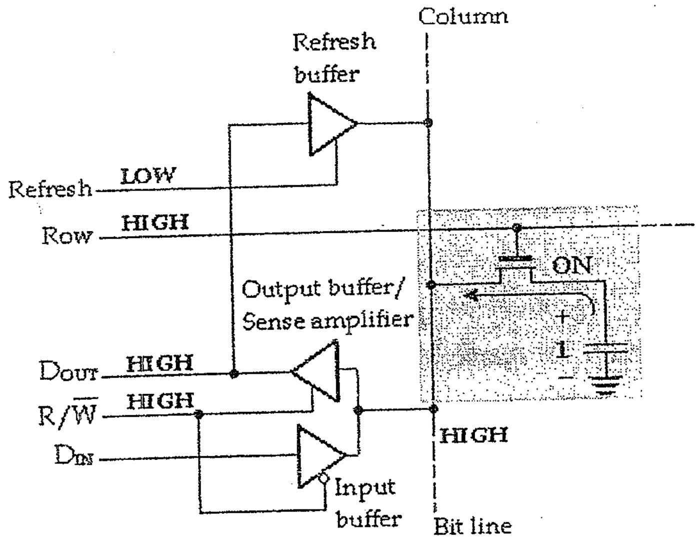
(a) Writing a 1 into the memory cell



(b) Writing a 0 into the memory cell

(ii) **Read:**

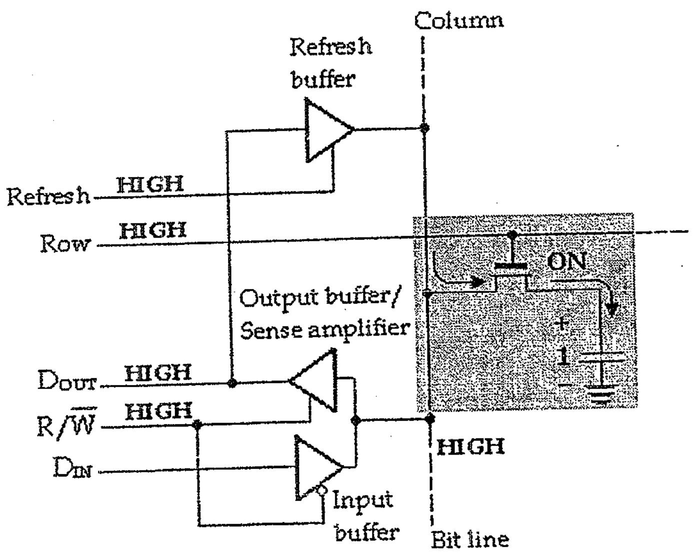
To read data from the cell, the R/W′ line is made HIGH, which enables output buffer and disables input buffer. When the row line is made HIGH, the transistor turns ON and connects the capacitor to the DOUT line through output buffer.



Reading a 1 from the memory cell

(iii) Refresh:

For refreshing the memory cell, the R/W line is HIGH, the row line is HIGH, and the refresh line is HIGH. The transistor turns on, connecting the capacitor to the bit line. The output buffer is enabled, and the stored data bit is applied to the input of the refresh buffer, which is enabled by the HIGH on the refresh input. This produces a voltage on the bit line corresponding to the stored bit thus refreshing the capacitor.



Refreshing a stored 1

2.6 Read- Only Memories (ROMs)

A ROM contains permanently or semi-permanently stored data, which can be read from the memory but either cannot be changed at all or cannot be changed without specialization equipment. A ROM stores data that are used repeatedly in system applications, such as tables, conversions, or programmed instructions for system initialization and operation. ROMs retain stored data when the power is OFF and are therefore nonvolatile memories.

The ROMs are classified as follows:

i. Masked ROM (ROM)

ii. Programmed ROM (PROM)

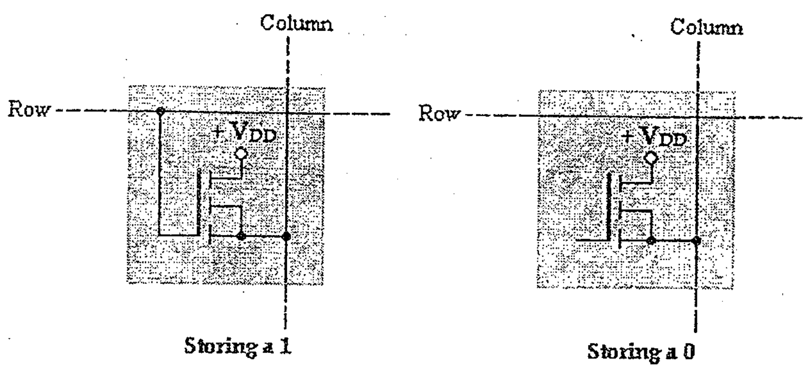
iii. Erasable PROM (EPROM)

iv. Electrically Erasable PROM (EEPROM)

1. Masked ROM

The mask ROM is usually referred to simply as a ROM. It is permanently programmed during the manufacturing process to provide widely used standard functions, such as popular conversions, or to provide user-specified functions. Once the memory is programmed, it cannot be changed.

Most IC ROMs utilize the presence or absence of a transistor connection at a row/column junction to represent a 1 or a 0. The presence of a connection from a row line to the gate of a transistor represents a 1 at that location because when the row line is taken HIGH; all transistors with a gate connection to that row line turn on and connect the HIGH (1) to the associated column lines.



ROM Cells

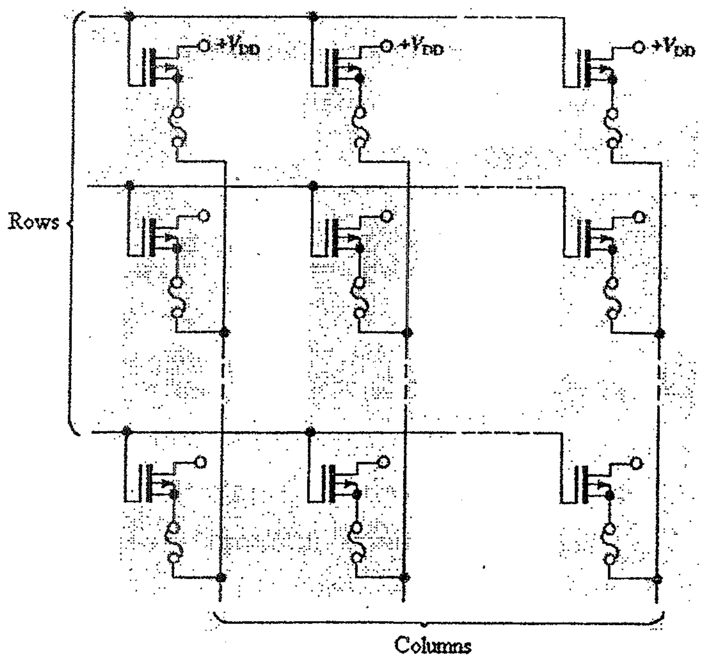
At row/column junctions where there are no gate connections, the column lines remain LOW (0) when the row is addressed.

PROM (Programmable Read-Only Memory)

The PROM (Programmable Read-only memory), comes from the manufacturer unprogrammed and are custom programmed in the field to meet the user's needs.

A PROM uses some type of fusing process to store bits, in which a memory link is burned open or left intact to represent a 0 or a 1. The fusing process is irreversible; once a PROM is programmed, it cannot be changed.

The fusible links are manufactured into the PROM between the source of each cell's transistor and its column line. In the programming process, a sufficient current is injected through the fusible link to bum it open to create a stored O. The link is left intact for a stored 1. All drains are commonly connected to V_{DD}.



PROM array with fusible links

Three basic fuse technologies used in PROMs are metal links, silicon links, and pn junctions. A brief description of each of these follows.

1. **Metal links** are made of a material such as *nichrome.* Each bit in the memory array is represented by a separate link. During programming, the link is either "blown" open or left intact. This is done basically by first addressing a given cell and then forcing a sufficient amount of current through the link to cause it to open. When the fuse is intact, the memory cell is configured as a logic 1 and when fuse is blown (open circuit) the memory cell is logic 0.

2. **Silicon links** are formed by narrow, notched strips of ***polycrystalline silicon.*** Programming of these fuses requires melting of the links by passing a sufficient amount of current through them. This amount of current causes a high temperature at the fuse location that oxidizes the silicon and forms insulation around the now-open link.

3. **Shorted junction,** or avalanche-induced migration, technology consists basically of two pn junctions arranged back-to-back. During programming, one of the diode junctions is avalanched, and the resulting voltage and heat cause aluminum ions to migrate and short the junction. The remaining junction is then used as a forward- biased diode to represent a data bit.

iii EPROM (Erasable Programmable ROM)

An EPROM is an erasable PROM. Unlike an ordinary PROM, an EPROM can be reprogrammed if an existing program in the memory array is erased first.

An EPROM uses an NMOSFET array with an isolated-gate structure. The isolated transistor gate has no electrical connections and can store an electrical charge for indefinite periods of time. The data bits in this type of array are represented by the presence or absence of a stored gate charge. Erasure of a data bit is a process that removes the gate charge.

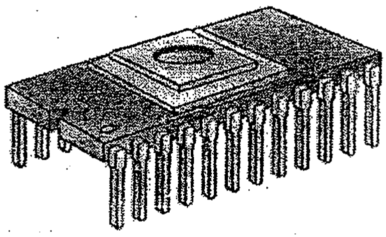
Two basic types of erasable PROMs are the ultraviolet erasable PROM (UV EPROM) and the electrically erasable PROM (EEPROM).

- UV EPROM:

You can recognize the UV EPROM device by the transparent quartz lid on the package, as shown in Figure below. The isolated gate in the FET of an ultraviolet EPROM is "floating" within an oxide insulating material. The programming process causes electrons to be removed from the floating gate. Erasure is done by exposure of the memory array chip to high-intensity ultraviolet radiation through the quartz window on top of the package.

The positive charge stored on the gate is neutralized after several minutes to an hour of exposure time. In EPROM's, it is not possible to erase selective information, when erased the entire information is lost. The chip can be reprogrammed.

It is ideally suited for product development, college laboratories, etc.



Ultraviolet Erasable PROM

During programming, address and datas are applied to address and data pins of the EPROM. The program pulse is applied to the program input of the EPROM. The program pulse duration is around 50msec and its amplitude depends on EPROM IC. It is typically 11.5V to 25V.

In EPROM, it is possible to program any location at any time- either individually, sequentially or at random.

IV * **EEPROM (Electrically Erasable PROM)**

The EEPROM (Electrically Erasable PROM), also uses MOS circuitry. Data is stored as charge or no charge on an insulating layer, which is made very thin (< 200Å). Therefore a voltage as low as 20- 25V can be used to move charges across the thin barrier in either direction for programming or erasing ROM.

An electrically erasable PROM can be both erased and programmed with electrical pulses. Since it can be both electrically written into and electrically erased, the EEPROM can be rapidly programmed and erased in-circuit for reprogramming.

It allows selective erasing at the register level rather than erasing all the information, since the information can be changed by using electrical signals.

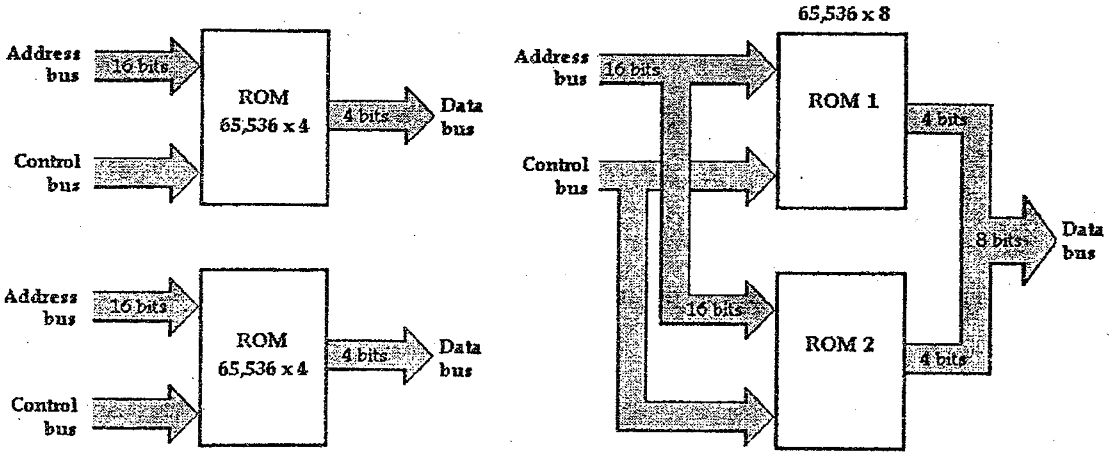
It has chip erase mode by which the entire chip can be erased in 10 msec. Hence EEPROM's are most expensive.

MEMORY EXPANSION

Available memory can be expanded to increase the word length (number of bits in each address) or the word capacity (number of different addresses) or both. Memory expansion is accomplished by adding an appropriate number of memory chips to the address, data, and control buses.

Word Length Expansion

To increase the word length of a memory, the number of bits in the data bus must be increased. An 8-bit word length can be achieved by using two memories each with 4-bit words as illustrated in Figure below. The 16-bit address bus is commonly connected to both memories so that the combination memory still has the same number of addresses (2^{16} = 65,536) as each individual memory. The 4-bit data buses from the two memories are combined to form an 8-bit data bus. Now when an address is selected, eight bits are produced on the data bus-four from each ROM.



Two separate 65, 536 x 4 ROMs

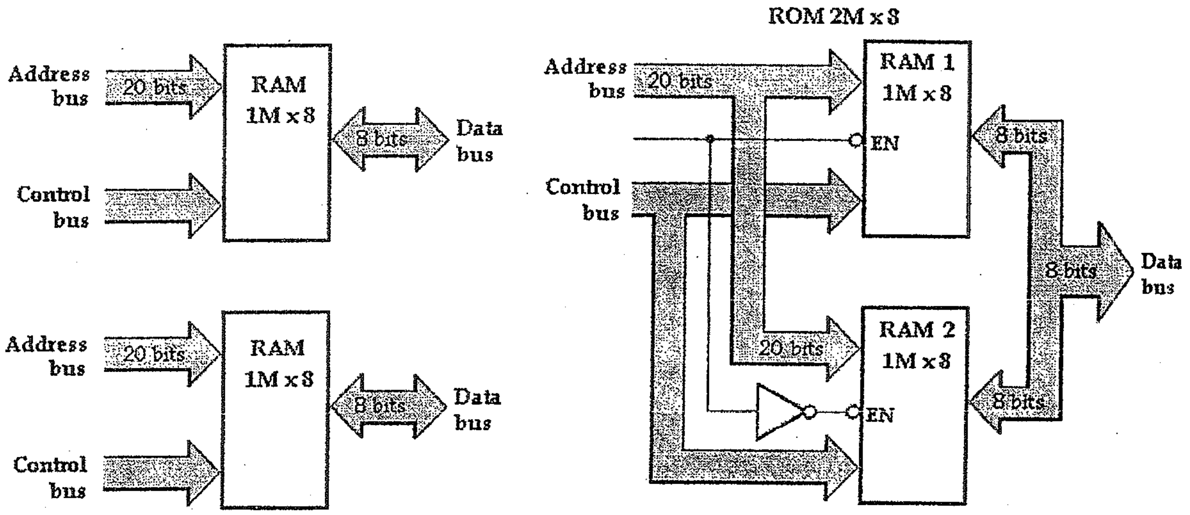
(b) One 65,536 x 8 ROM from two 65, 536 x 4 ROMs

Illustrate of word-length expansion

Word-Capacity Expansion:

When memories are expanded to increase the word capacity, the number of addresses is increased. Two 1M x 8 RAMs are expanded to form a 2M x 8 memory is shown below.

Each individual memory has 20 address bits to select its 1,048,576 addresses. The expanded memory has 2,097,152 addresses and therefore requires 21 address bits, as shown in part (b). The twenty-first address bit is used to enable the appropriate memory chip. The data bus for the expanded memory remains eight bits wide.



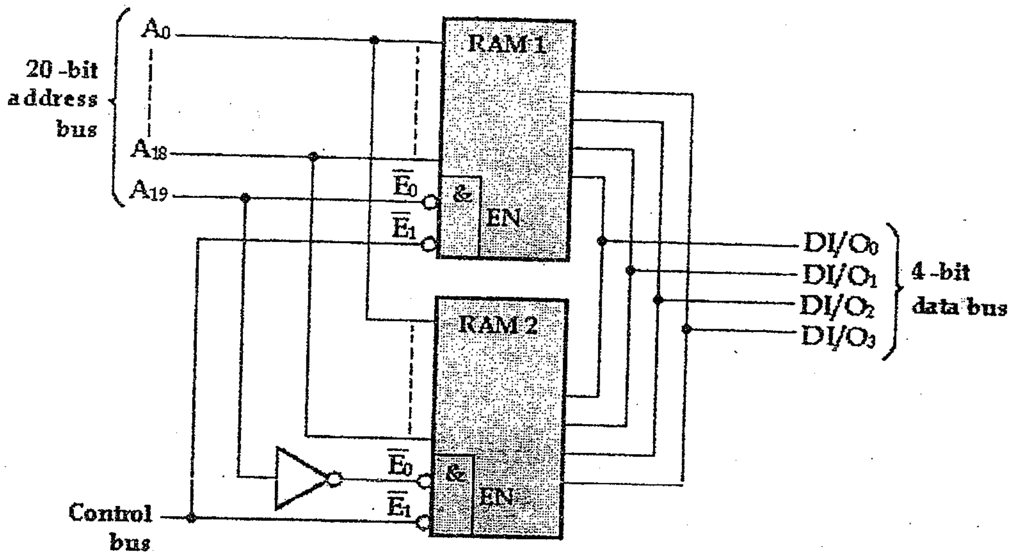
(a) Individual memories each store RAM 1,048,576 8-bit words **(b) Memories expanded to form a 2M x 8 requiring a 21-bit address bus**

Word capacity Expansion

1. Use 512k x 4 RAMs to implement a 1M x 4 memory.

The expanded addressing is achieved by connecting the chip enable (E_o') input to the twentieth address bit (A_{19}). Input (E_1') is used as an enable input common to both memories. When the twentieth address bit (A_{19}) is LOW, RAM 1 is selected (RAM 2 is disabled), and the nineteen lower-order address bits (A_0 –A_{18}) access each of the addresses in RAM 1. When the twentieth address bit (A_{19}) is

HIGH, RAM 2 is enabled by a LOW on the inverter output (RAM 1 is disabled), and the nineteen lower-order address bits ($A_0 - A_{18}$) access each of the RAM 2 addresses.



1M x 4 RAM using 512K x 4 RAM

Advantages of RAM:

1. Fast operating speed (< 150 nsec),
2. Low power dissipation (< 1mW),
3. Economy,
4. Compatibility,
5. Non-destructive read-out.

Advantages of ROM:

1. Ease and speed of design,
2. Faster than MSI devices (PLD and FPGA)
3. The program that generates the ROM contents can easily be structured to handle unusual or undefined cases,
4. A ROM's function is easily modified just by changing the stored pattern, usually without changing any external connections,
5. More economical.

Disadvantages of ROM:

1. For functions more than 20 inputs, a ROM based circuit is impractical because of the limit on ROM sizes that are available.
2. For simple to moderately complex functions, ROM based circuit may be costly: consume more power; run slower.

Comparison between RAM and ROM:

S.No	RAM	ROM
1	RAMs have both read and write capability.	ROMs have only read operation.
2	RAMs are volatile memories.	ROMs are non-volatile memories.
3	They lose stored data when the power is turned OFF.	They retain stored data even if power is turned off.
4	RAMs are available in both bipolar and MOS technologies.	RAMs are available in both bipolar and MOS technologies.
5	Types: SRAM, DRAM, EEPROM	Types: PROM, EPROM.

Comparison between SRAM and DRAM:

S.No	Static RAM	Dynamic RAM
1	It contains less memory cells per unit area.	It contains more memory cells per unit area.
2	Its access time is less, hence faster memories.	Its access time is greater than static RAM
3	It consists of number of flip-flops. Each flip-flop stores one bit.	It stores the data as a charge on the capacitor. It consists of MOSFET and capacitor for each cell.
4	Refreshing circuitry is not required.	Refreshing circuitry is required to maintain the charge on the capacitors every time after every few milliseconds. Extra hardware is required to control refreshing.
5	Cost is more	Cost is less.

Comparison of Types of Memories:

Memory type	Non- Volatile	High Density	One- Transistor cell	In-system writability
SRAM	No	No	No	Yes
DRAM	No	Yes	Yes	Yes
ROM	Yes	Yes	Yes	No
EPROM	Yes	Yes	Yes	No
EEPROM	Yes	No	No	Yes

PROGRAMMABLE LOGIC DEVICES:

INTRODUCTION:

A combinational PLD is an integrated circuit with programmable gates divided into an AND array and an OR array to provide an AND-OR sum of product implementation. The PLD's can be reprogrammed in few seconds and hence gives more flexibility to experiment with designs. Reprogramming feature of PLDs also makes it possible to accept changes/modifications in the previously design circuits.

The advantages of using programmable logic devices are:

1. Reduced space requirements.
2. Reduced power requirements.
3. Design security.
4. Compact circuitry.
5. Short design cycle.
6. Low development cost.
7. Higher switching speed.
8. Low production cost for large-quantity production.

According to architecture, complexity and flexibility in programming in PLD's are classified as –

- PROMs : Programmable Read Only memories,

- PLAs : Programmable Logic Arrays,
- PAL : Programmable Logic Array,
- FPGA : Field Programmable Gate Arrays,
- CPLDs : Complex Programmable Logic Devices.

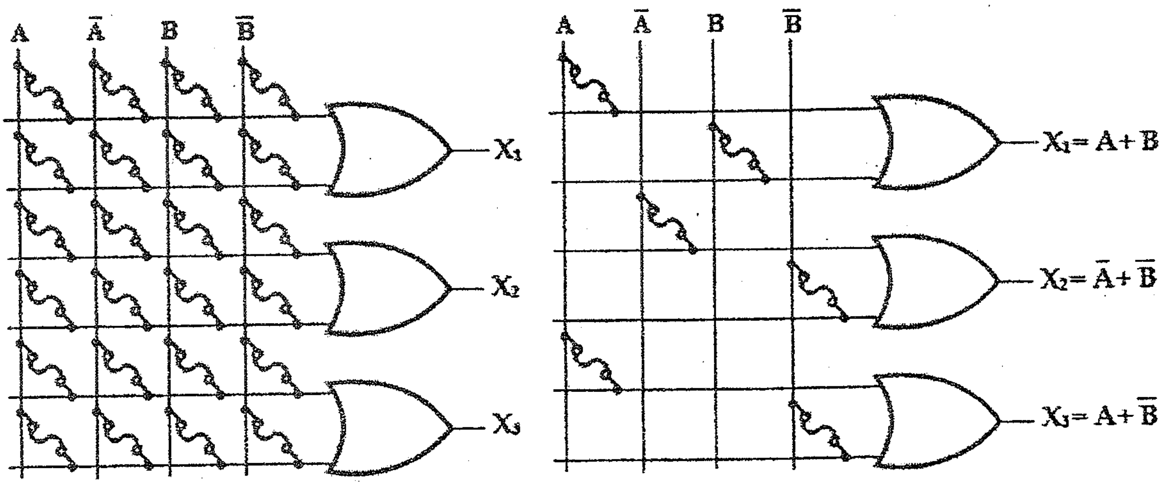
Programmable Arrays:

All PLDs consists of programmable arrays. A programmable array is essentially a grid of conductors that form rows and columns with a fusible link at each cross point. Arrays can be either fixed or programmable.

The OR Array:

It consists of an array of OR gates connected to a programmable matrix with fusible links at each cross point of a row and column, as shown in the figure below. The array can be programmed by blowing fuses to eliminate selected variables from the output functions. For each input to an OR gate, only one fuse is left intact in order to connect the desired variable to the gate input. Once the fuse is blown, it cannot be reconnected.

Another method of programming a PLD is the antifuse, which is the opposite of the fuse. Instead of a fusible link being broken or opened to program a variable, a normally open contact is shorted by "melting" the antifuse material to form a connection.



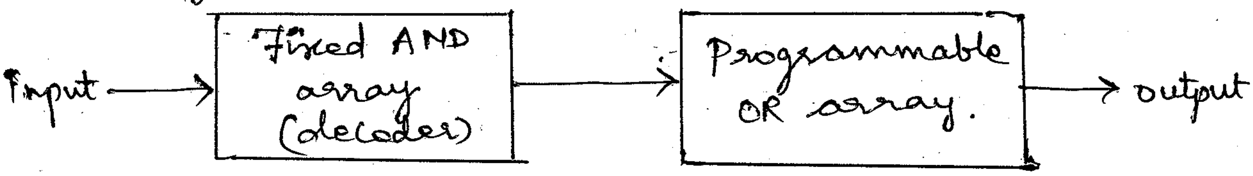
(a) Unprogrammed (b) Programmed

An example of a basic programmable OR array

PROGRAMMABLE LOGIC DEVICES.

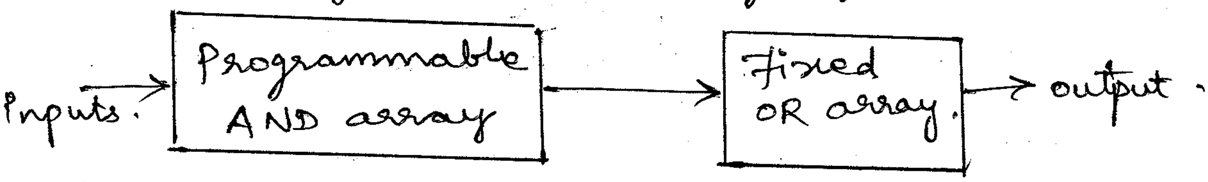
* A Combinational PLD is an integrated circuit with programmable gates divided into an AND array and an OR array to provide an AND-OR sum of product implementation.
* There are three major types of combinational PLDs and they differ in the placement of programmable connections is AND-OR array.

Programmable read-only memory (PROM).



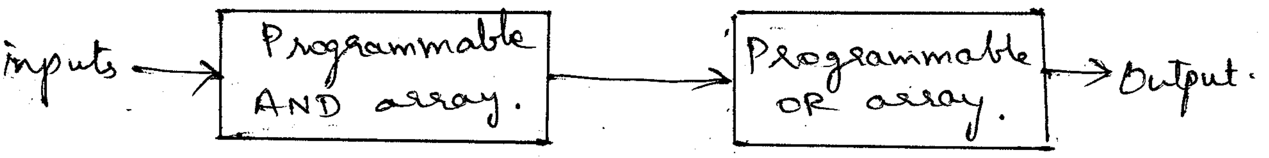
The programmable read-only memory has a fixed AND array constucted as a decoder and programmable OR array. The programmable OR gates implement the Boolean functions is sum of minterms.

Programmable Array logic (PAL).



Programmable array logic has a programmable AND array and a fixed OR array. The AND gates are programmed to provide the product terms for the boolean functions which are logically summed in each OR gate.

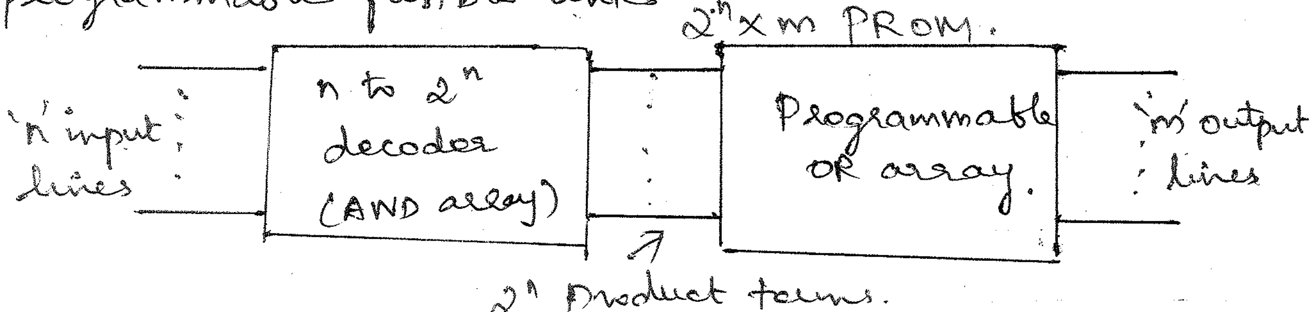
Programmable logic array (PLA).



The most flexible PLD is programmable logic array where both AND and OR arrays can be programmed. The product terms in AND array may be shared by any OR gate to provide the required sum of product implementation.

PROGRAMMABLE ROM:

* used for code conversions, generating bit patterns for characters and as look-up tables for arithmetic functions.
* Consist of fixed AND-array and a programmable OR array. The AND array is an n to 2^n decoder and the OR array is simply a collection of programmable OR gates. The OR array is also called memory array.
* The decoder serves as a minterm generator.
* The n-variable minterms appear on the 2^n lines at the decoder output. The 2^n outputs are connected to each of the 'm' gates in the OR array through programmable fusible links.



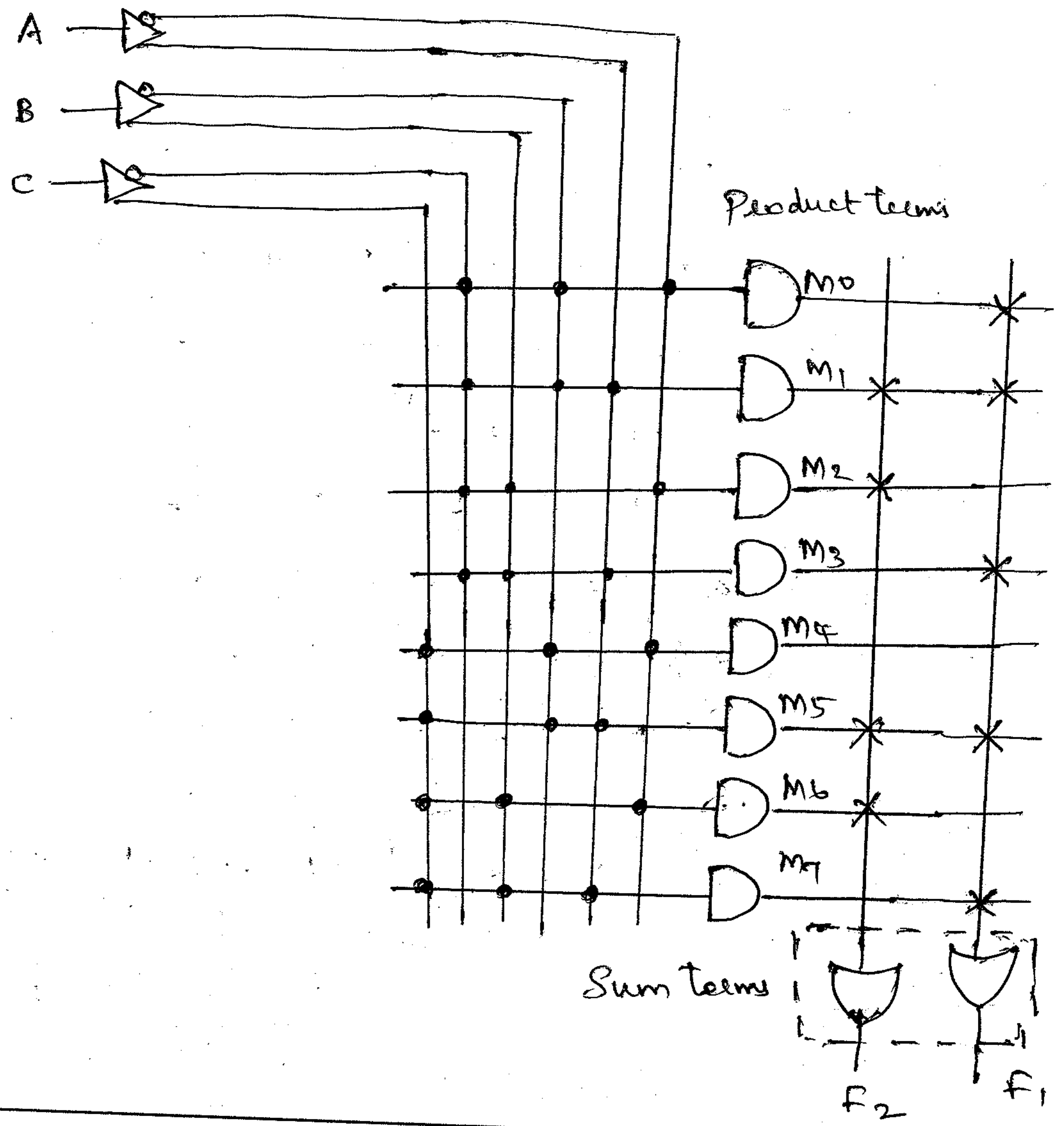
1. Using PROM realize the following expression.

$$f_1(A,B,C) = \sum m(0,1,3,5,7)$$

$$f_2(A,B,C) = \sum m(1,2,5,6)$$

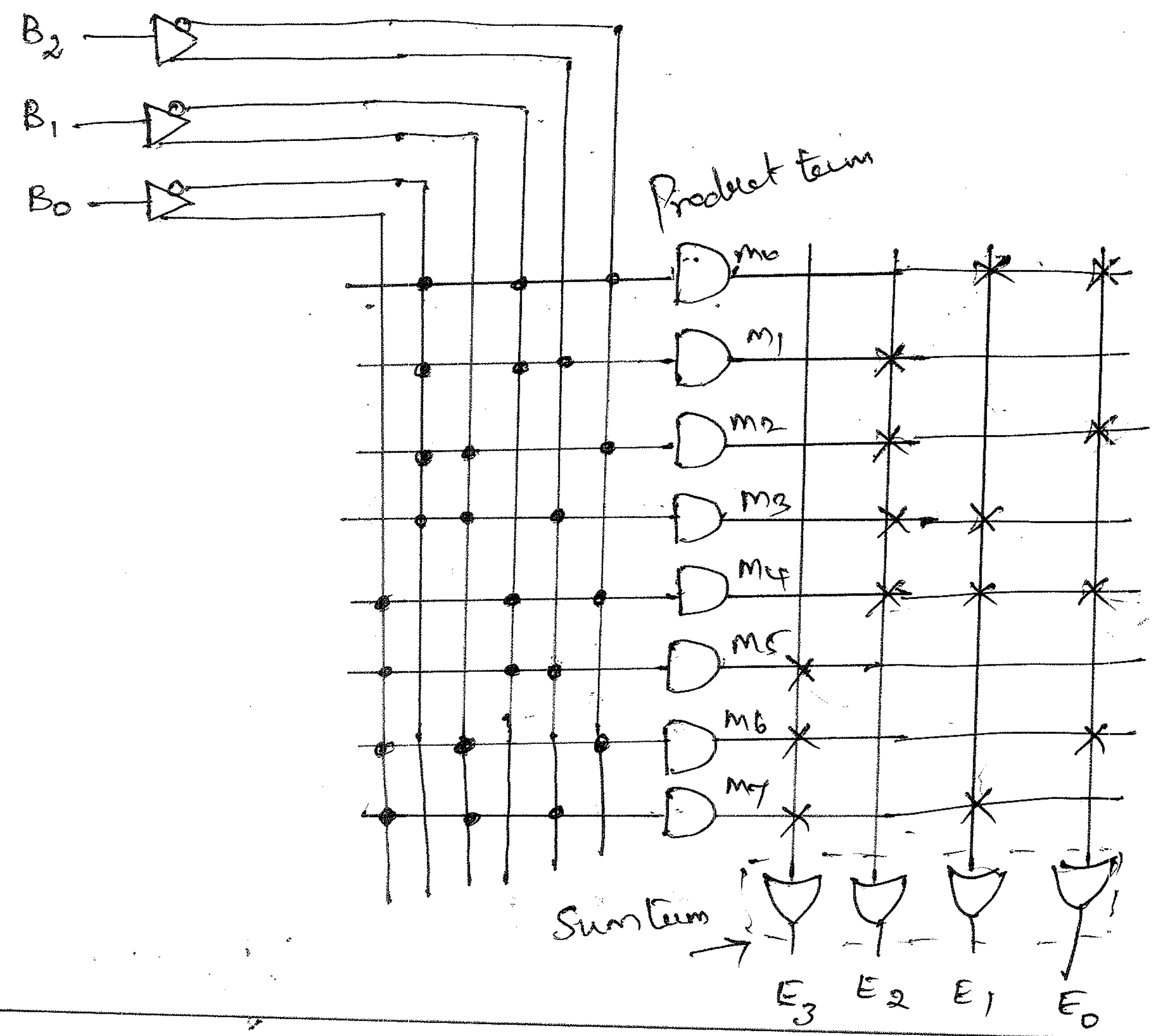
Truth table.

A	B	C	F1	F2
0	0	0	1	0
0	0	1	1	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	0
1	0	1	1	1
1	1	0	0	1
1	1	1	1	0



2. Design a combinational circuit using PROM. The circuit accepts 3-bit binary and generates its equivalent excess-3 code.

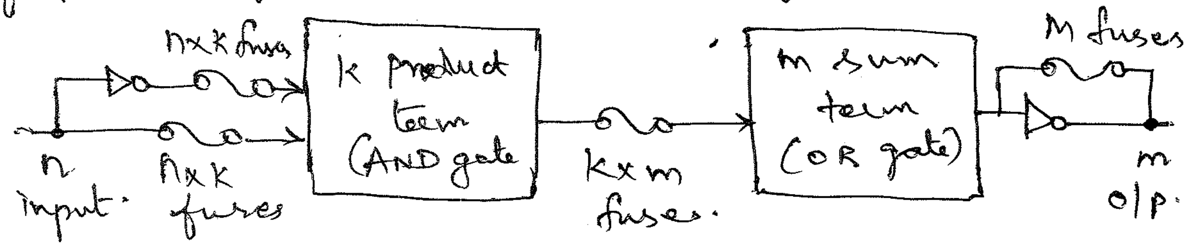
B_2	B_1	B_0	E_3	E_2	E_1	E_0
0	0	0	0	0	1	1
0	0	1	0	1	0	0
0	1	0	0	1	0	1
0	1	1	0	1	1	0
1	0	0	0	1	1	1
1	0	1	1	0	0	0
1	1	0	1	0	0	1
1	1	1	1	0	1	0



PROGRAMMABLE LOGIC ARRAY (PLA).

The PLA is similar to PROM except that PLA doesnot provide full coding of variable and doesnot generate all minterms.

The decoder is replaced by an array of AND gates that can be programmed to generate any product term of input variables. The product terms are then connected to OR gate to provide the sum of product for required boolean functions.



1. Implement the combinational circuit with a PLA having 3 inputs, 4 product terms and 2 outputs for the functions. $f_1(A,B,C) = \Sigma m(0,1,2,4)$

$f_2(A,B,C) = \Sigma m(0,5,6,7)$.

Truth table

A B C	F_1	F_2
0 0 0	1	1
0 0 1	1	0
0 1 0	1	0
0 1 1	0	0
1 0 0	1	0
1 0 1	0	1
1 1 0	0	1
1 1 1	0	1

K-map simplification

A \ BC	00	01	11	10
0	1 (0)	1 (1)	0 (3)	1 (2)
1	1 (4)	0 (5)	0 (7)	0 (6)

$f_1 = A'B' + A'C' + B'C'$.

A \ BC	00	01	11	10
0	1 (0)	0 (1)	0 (3)	0 (2)
1	0 (4)	1 (5)	1 (7)	1 (6)

$f_2 = AC + AB + A'B'C'$.

A \ BC	00	01	11	10
0	1 (0)	(1)	0 (3)	1 (2)
1	1 (4)	0 (5)	0 (7)	0 (6)

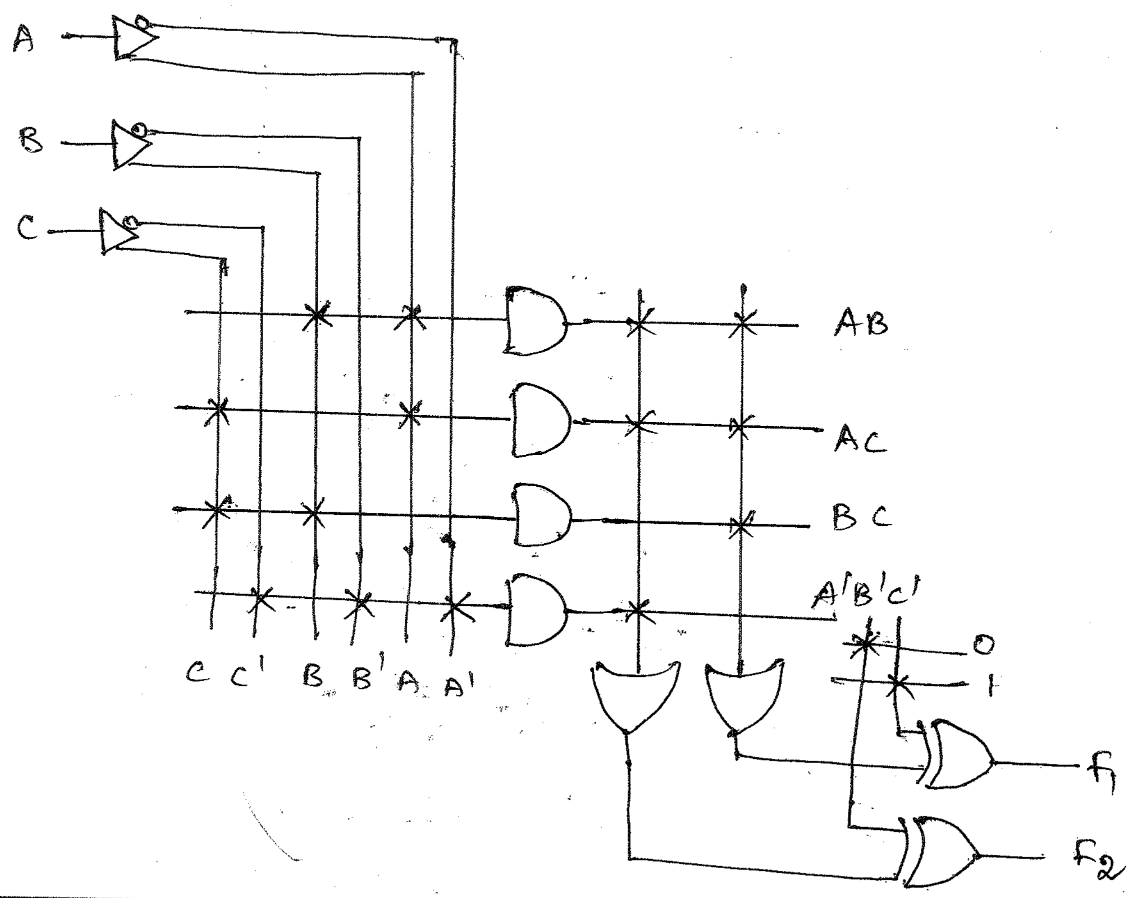
$f_1' = AC + BC + AB$.

A \ BC	00	01	11	10
0	(0)	0 (1)	0 (3)	0 (2)
1	0 (4)	(5)	(7)	(6)

$f_2' = A'C + A'B + AB'C'$.

Program table

	Product term	Inputs A	B	C	Output $F_1(C)$	$F_2(T)$
AB	1	1	1	–	1	1
AC	2	1	–	1	1	1
BC	3	–	1	1	1	–
$A'B'C'$	4	0	0	0	–	1



2. Implement the following function using PLA

$f_1(A,B,C) = \sum m(1,2,4,6)$

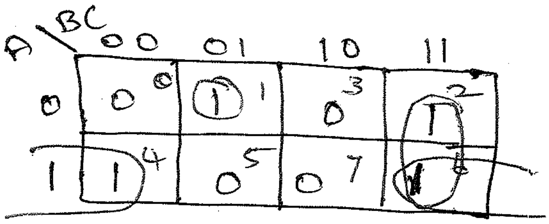
$F_2(A,B,C) = \sum m(0,1,6,7)$

$F_3(A,B,C) = \sum m(2,6)$

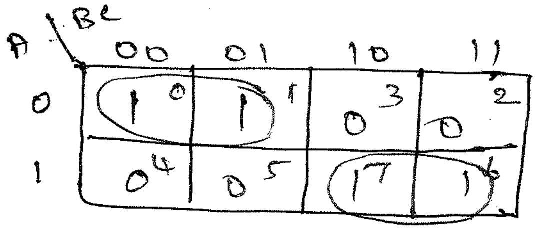
Truth table

A B C	f_1	f_2	f_3
0 0 0	0	1	0
0 0 1	1	1	0
0 1 0	1	0	1
0 1 1	0	0	0
1 0 0	1	0	0
1 0 1	0	0	0
1 1 0	1	1	1
1 1 1	0	1	0

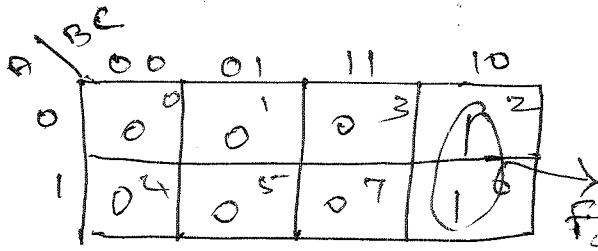
K map simplification



$f_1 = A'B'C + AC' + BC'$



$F_2 = A'B' + AB$

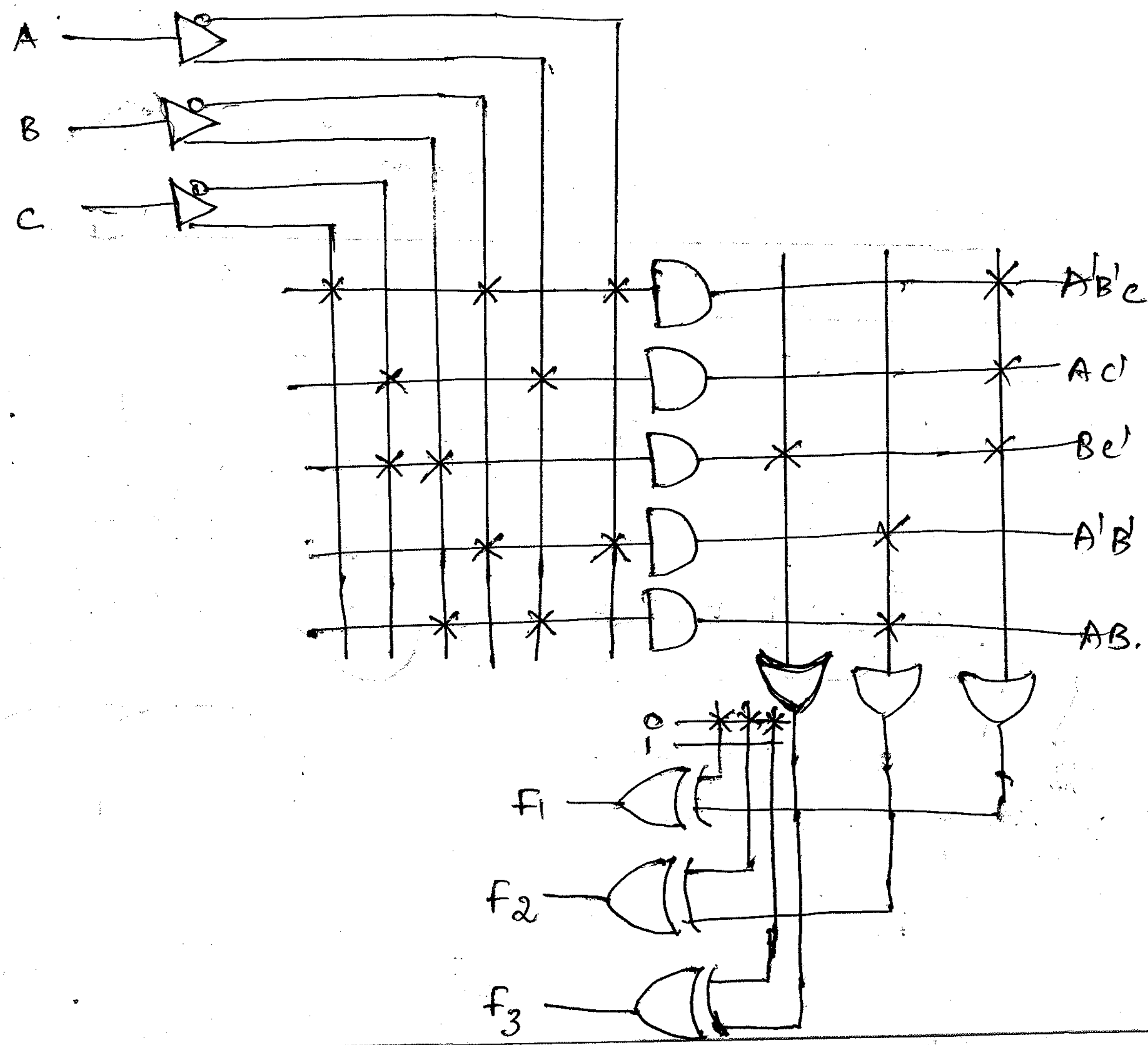


$F_3 = BC'$

Program table.

	Product term	Inputs			outputs		
		A	B	C	F1(T)	F2(T)	F3(T)
A'B'C	1	0	0	1	1	–	–
AC'	2	1	–	0	1	–	–
BC'	3	–	1	0	1	–	1
A'B'	4	0	0	–	–	1	–
AB	5	1	1	–	–	1	–

PLA diagram



3. Design a BCD to excess-3 code converter and implement using suitable PLA.

Truth table.

BCD code.				Excess-3 code.			
B_3	B_2	B_1	B_0	E_3	E_2	E_1	E_0
0	0	0	0	0	0	1	1
0	0	0	1	0	1	0	0
0	0	1	0	0	1	0	1
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	1
0	1	0	1	1	0	0	0
0	1	1	0	1	0	0	1
0	1	1	1	1	0	1	0
1	0	0	0	1	0	1	1
1	0	0	1	1	1	0	0

K-map simplification

For E_3

$B_3B_2 \backslash B_1B_0$	00	01	11	10
00	0	0	0	0
01	0	1	1	1
11	X	X	X	X
10	1	1	X	X

$E_3 = B_3 + B_2B_0 + B_2B_1$

For E_2

$B_3B_2 \backslash B_1B_0$	00	01	11	10
00	0	1	1	1
01	1	0	0	0
11	X	X	X	X
10	0	1	X	X

$E_2 = B_2B_1'B_0' + B_2'B_0 + B_2'B_1$.

For E_1

$B_3B_2 \backslash B_1B_0$	00	01	11	10
00	1	0	1	0
01	1	0	1	0
11	X	X	X	X
10	1	0	X	X

$E_1 = B_1'B_0' + B_1B_0$

For E_0.

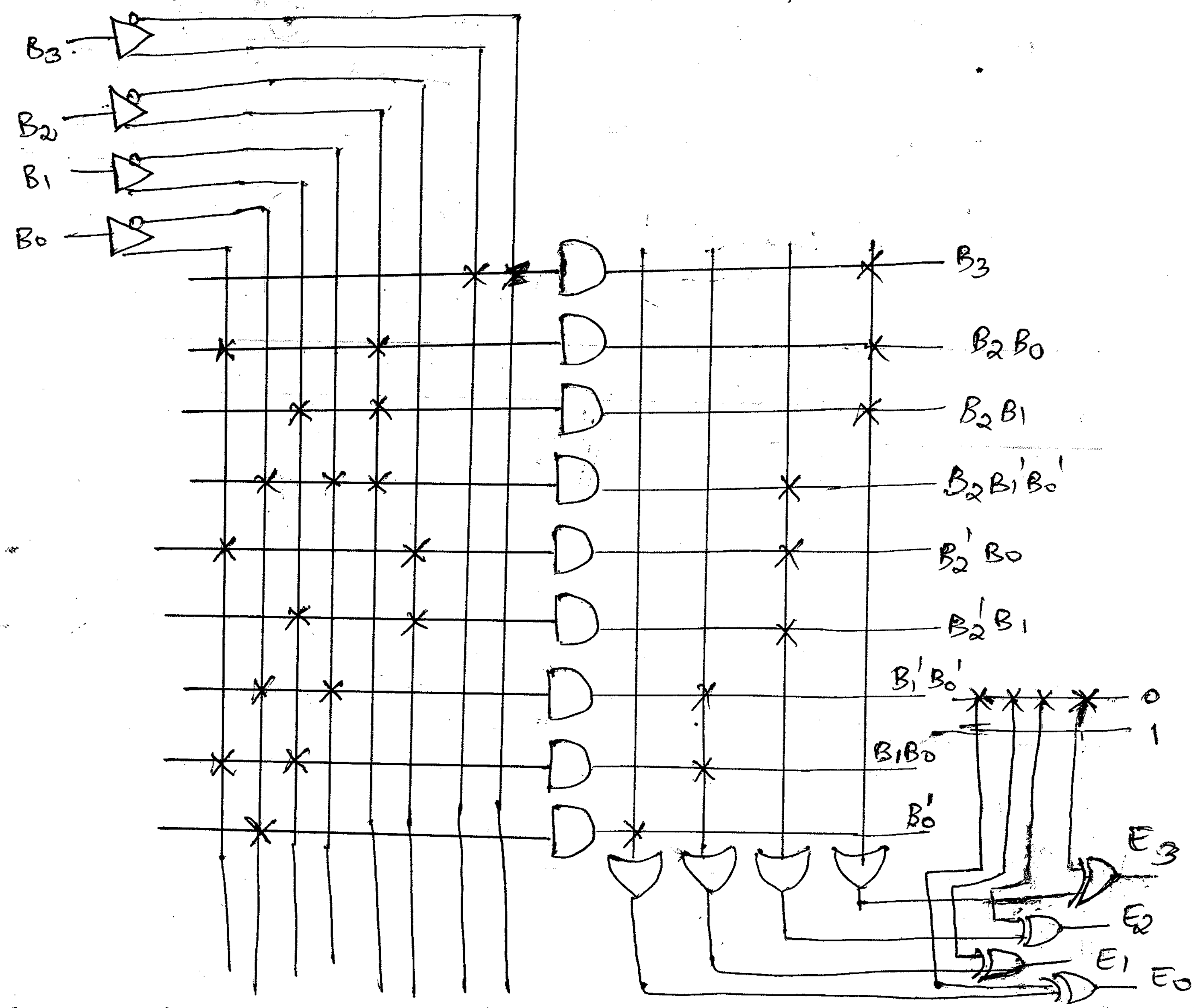
$B_3B_2 \backslash B_1B_0$	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	X	X	X	X
10	1	0	X	X

$E_0 = B_0'$

Program table.

	Product term	Inputs				Outputs			
		B_3	B_2	B_1	B_0	E_3(T)	E_2(T)	E_1(T)	E_0(T)
B_3	1	1	–	–	–	1	–	–	–
$B_2 B_0$	2	–	1	–	1	1	–	–	–
$B_2 B_1$	3	–	1	1	–	1	–	–	–
$B_2 B_1' B_0'$	4	–	1	0	0	–	1	–	–
$B_2' B_0$	5	–	0	–	1	–	1	–	–
$B_2' B_1$	6	–	0	1	–	–	1	–	–
$B_1' B_0'$	7	–	–	0	0	–	–	1	–
$B_1 B_0$	8	–	–	1	1	–	–	1	–
B_0'	9	–	–	–	0	–	–	–	1

PLA diagram.



Programmable array logic (PAL).

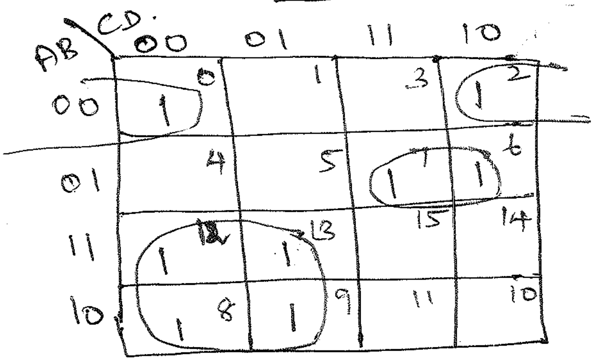
$w(A,B,C,D) = \Sigma(0,2,6,7,8,9,12,13)$

$x(A,B,C,D) = \Sigma(0,2,6,7,8,9,12,13,14)$

$y(A,B,C,D) = \Sigma(2,3,8,9,10,12,13)$

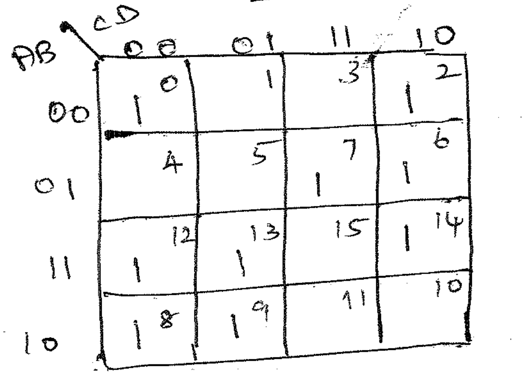
$z(A,B,C,D) = \Sigma(1,3,4,6,9,12,14)$

For w



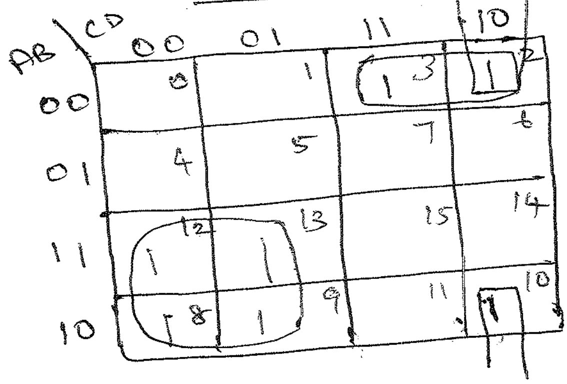
$w = \bar{A}\bar{B}\bar{D} + \bar{A}BC + A\bar{C}$

For x



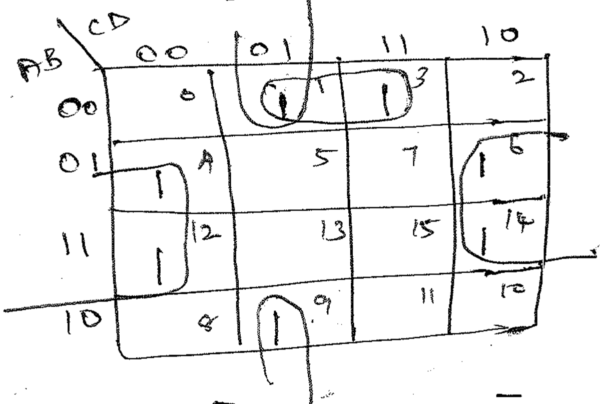
$x = \bar{A}\bar{B}\bar{D} + \bar{A}BC + A\bar{C} + BC\bar{D}$

For y



$y = \bar{A}\bar{B}C + \bar{B}C\bar{D} + A\bar{C}$

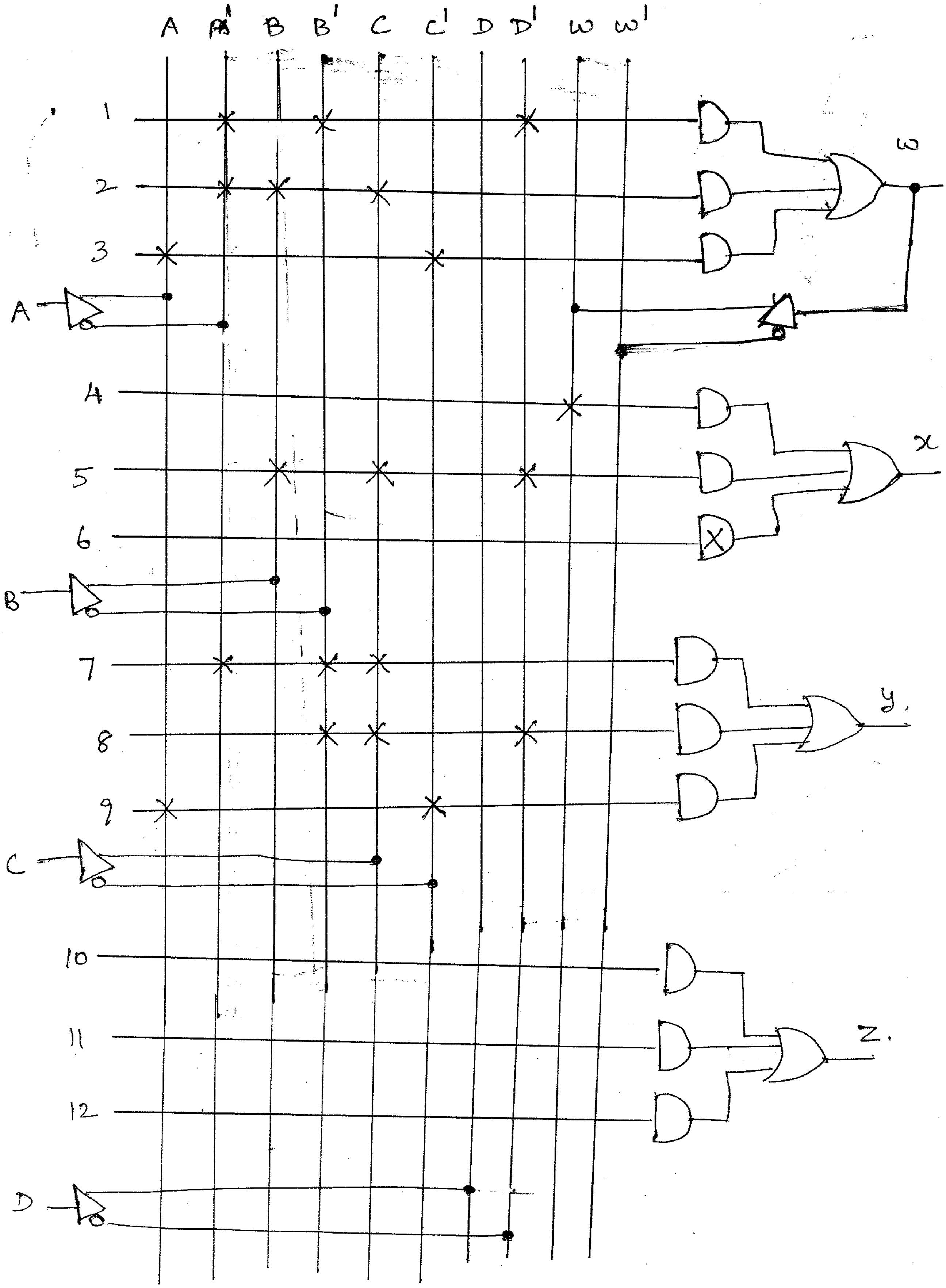
For z



$z = \bar{A}\bar{B}D + \bar{B}\bar{C}D + B\bar{D}$

Product terms	AND inputs					outputs
	A	B	C	D	w	
1. $\bar{A}\bar{B}\bar{D}$	0	0	–	0	–	$w = \bar{A}\bar{B}\bar{D} + \bar{A}BC + A\bar{C}$
2. $\bar{A}BC$	0	1	1	–	–	
3. $A\bar{C}$	1	–	0	–	–	
4. w	–	–	–	–	1	$x = w + BC\bar{D}$
5. $BC\bar{D}$	–	1	1	0	–	
6. –	–	–	–	–	–	
7. $\bar{A}\bar{B}C$	0	0	1	–	–	$y = \bar{A}\bar{B}C + \bar{B}C\bar{D} + A\bar{C}$
8. $\bar{B}C\bar{D}$	–	0	1	0	–	
9. $A\bar{C}$	1	–	0	–	–	
10. $\bar{A}\bar{B}D$	0	0	–	1	–	$z = \bar{A}\bar{B}D + \bar{B}\bar{C}D + B\bar{D}$.
11. $\bar{B}\bar{C}D$	–	0	0	1	–	
12. $B\bar{D}$	–	1	–	0	–	

PAL diagram.



DIGITAL LOGIC FAMILIES

I)Fundamental characteristics of Logic families

1. **Fan-in:** the fan in of a gate is the number of inputs connected to the gate without any degradation in the voltage levels. For example: an inverter has fan-in of 1, two input NOR gate, fan-in 2. etc., the propagation delay increases with increase in fan in i.e., 2 input gates is faster than 4 input gates. Fan-in of gate should be selected to accommodate the number of inputs.
2. **Fan-out:** the number of load gates that a logic gate output is capable of driving without possible logic errors.

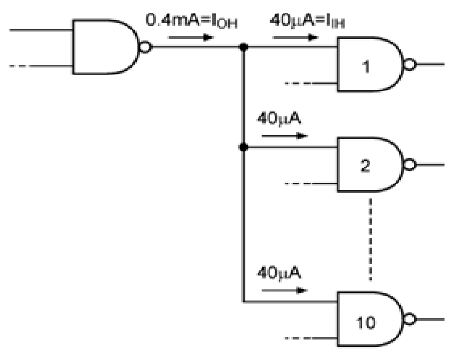


Fig. High level output

It provides a current source I_{OH} to all the gate inputs connected to it. Each gate input requires a current I_{IH} for proper operation.

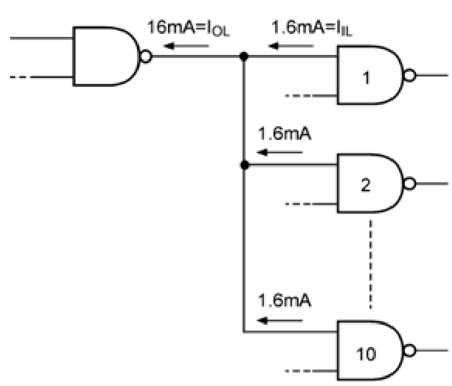


Fig. Low level output

It provides a current sink I_{OL} for all the gate inputs connected to it. Each gate input supplies a current I_{IL}.

FAN OUT = $\frac{I_{OH}}{I_{IL}}$ or $\frac{I_{OL}}{I_{IL}}$ (for TTL fan-out=10(max))

3. **Power dissipation:**

The power dissipation represents the amount of power needed by the gate and is expressed in milliwatts (mW). This number represents he power delivered to the gate from power supply. It is defined as the amount of power that is dissipated in gate is calculated from the supply voltage V_{CC} and the current I_{CC} that is drawn by the circuit P= V_{CC} . I_{CC}

$$I_{CC(avg)}=\frac{I_{CCH}+I_{CCL}}{2}$$

I_{CCH} → current drawn from the power supply when the output of gate is in high-voltage level

I_{CCL} → when the output of gate is in low-voltage level

Average power dissipated $P_D = I_{CC(avg)} \cdot V_{CC}$

Example: A standard TTL NAND gate uses a supply voltage V_{CC} of 5V and has current drains I_{CCH}=1mA, I_{CCL}=3 mA. Find the power dissipated for 4 NAND gate.

$$I_{CC(avg)}=\frac{I_{CCH}+I_{CCL}}{2}$$

$$=\frac{3m+1m}{2}=2mA$$

$$P_{dissipated}= I_{CC(avg)} \cdot V_{CC}$$

=2m x 5

=10mW

Power dissipated for 4 NAND gate=4 x 10m = 40 Mw

4. **Propagation delay:** the propagation delay of a gate is the average transition – delay time for the signal to propagate from input to output when the binary input signal changes in value. The signals through a gate take a certain amount of time to propagate from the inputs to the output. This interval of time is defined as the propagation delay of the gate. Propagation delay is measured in nanoseconds(ns).

$P_{delay} = \max(t_{PLH}, t_{PHL})$

The larger value is considered as a propagation delay time for that logic gates.

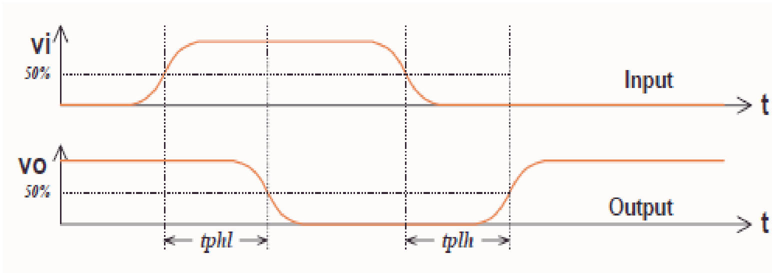


Fig. propagation delay

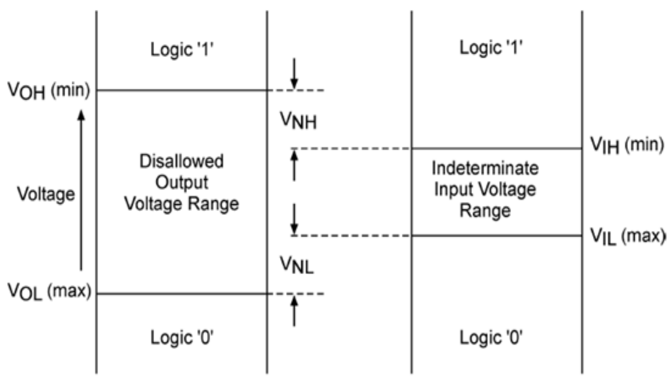
t_{PLH}: it is the delay time measured when output is charging from logic1 to logic 0 state (high to low)

t_{PHL}: it is the delay time measured when output is charging from logic 0 to logic 1 state(low to high)

5. Noise margin: the unwanted signals are called noise.

AC noise: random pulse caused by other switching signal

DC noise: by drift in voltage level of signal.



Output voltage range **input voltage range**

Fig. Noise margin

Noise margin is the maximum noise voltage added to an input signal of a digital circuit that does not cause an undesirable change in circuits output. The noise margin is the difference $V_{IL} - V_{OL}$, whichever is smaller.

II)SWITCHING CIRCUITS

1. **Semiconductor diode**

The diode behaves like 'one way' switch.

Diode is ON when forward biased ,switch is closed and therefore conducts current.

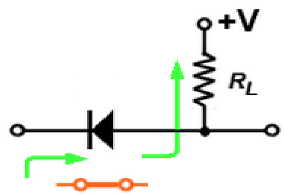


Fig. Diode as closed switch

Diode is OFF when it is reverse biased and switch is open and will not conduct current.

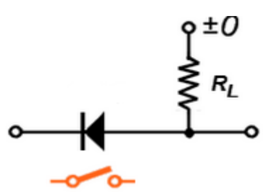
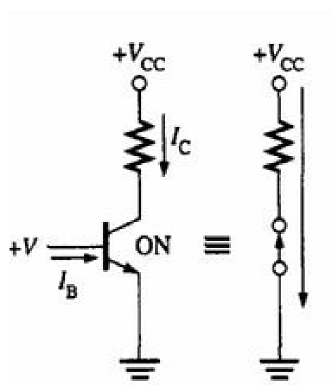


Fig. Diode as open switch

2. **BJT's:**

ON: working as saturated region (emitter base junction and collector base junction are forward biased)



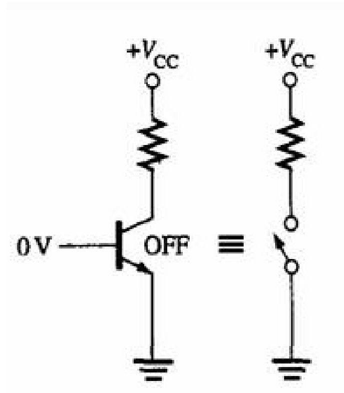
Note:

If input voltage through base is high (or) if input voltage through emitter transistor is low, these conditions makes the transistor to ON.

Fig. BJT as closed switch

High base turns the transistor ON and makes it as closed switch.

OFF: working as a cut off(emitter base junction and collector base junction are reverse biased)



Note:

If input voltage through emitter is high (or) if input voltage through base transistor is low, these conditions makes the transistor to OFF.

Fig. BJT as open switch

Low on base turns the transistor OFF and makes it an open switch.

III) <u>RESISTOR–TRANSISTOR LOGIC (RTL) CIRCUIT (NOR GATE)</u>

Resistor–transistor logic (RTL) uses resistors as the input network and bipolar junction transistors (BJTs) as switching devices. This has been used in early computers with electron tubes, and in RTL circuits constructed with discrete components, but in 1961 it became the first digital logic family to be produced as a monolithic integrated circuit. Such were used in the US space program in 1962.

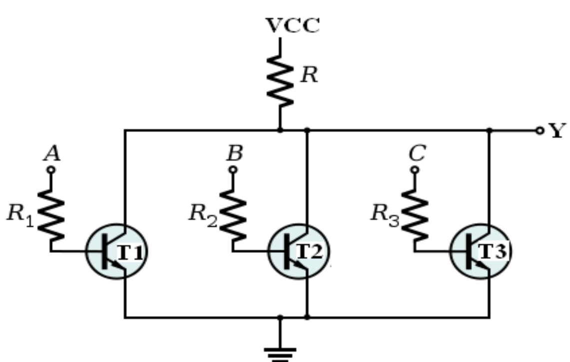


Fig. RTL circuit for NOR logic

Table. Truth table for 3 input NOR

INPUTS			OUTPUT
A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	0
1	0	1	0
1	1	0	0
1	1	1	0

All the binary inputs are given to the base of the transistor through a resistor and all the emitter terminal are grounded. All the collector terminals are tied together at the output.

Low level voltage: 0.2V

High level voltage: 1 to 3.6 V

Case i: If any input in RTL gate is high, the corresponding transistor is driven into saturation (switch closed) and output goes low.

Case ii: if all inputs are low at 0.2V, all transistors are cutoff (switch open) and the output goes high.

Advantage:

1. RTL technology involves a minimum number of transistors, which was an important consideration before integrated circuit technology (that is, in circuits using discrete components), as transistors were the most expensive component to produce.
2. Output loaded with input of other gate, more current is consumed by load.
3. Any voltage below 1V in the output may not drive the next transistor into saturation.
4. Propagation delay averages 25ns.

Limitations:

1. It has high power dissipation when the transistor is switched on (the power is dissipated mainly by the base resistors connected to logical "1" and by the collector resistor). This requires that more current be supplied to and heat be removed from RTL circuits.
2. It has limited fan-in: 3 inputs being the limit for many circuit designs, before it completely lost usable noise immunity
3. It has poor noise immunity, and limited ability to drive multiple loads (fan-out), so buffer circuits such as this were needed to expand the number of drivable stages, provide isolation, or drive bus lines.

IV)Transistor-Transistor Logic (TTL)

TTL is called as transistor transistor logic since the logic gating and amplifying function are done by transistors. In 1963, TTL integrated circuits were manufactured by several semiconductor companies like Texas instruments with the start of 5400 series and in 1964 with a series of 7400. TTL component parts are made by Motorola, Fairchild, Siemens, national semiconductors.TTL circuits were preferred with high speed and low power dissipation allows optimization of a design.

TTL is notable circuit which has a wide spread integrated circuits(IC) family, which is been used in many application such as computer industrial controls, test equipment and instrumentation, consumer electronics, synthesizers etc.,.

All TTL series are available in SSI components and in more complex forms, such as MSI and LSI components.TTL series differs by the internal construction of basic NAND gate but not in the performance.

Types based on output configuration

1. Open collector output
2. Totem-pole output
3. Three state output

1)Open collector output gate (TTL NAND gate)

An open collector device ia an IC with an output gate no connected to V_{CC}. Open collector IC consist of circuit with final driver unconnected atleast to V_{CC}. The input base to the driver is used to receive the signal, while the common pin emitter is grounded. Since collector is unattached, the lead could be attached to any circuit voltage to interface with another device.

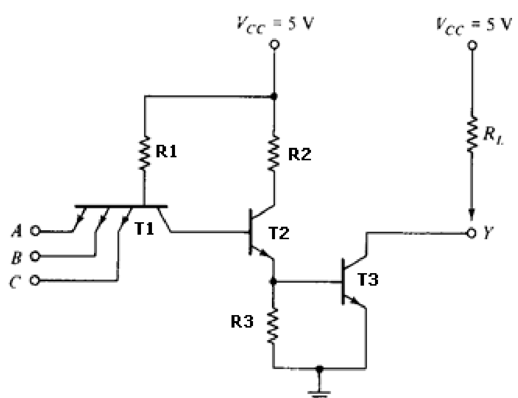


Table. Truth table for NAND

INPUTS			OUTPUT
A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Fig. Open collector output gate (TTL NAND logic)

Cut off mode:

The operating mode of a bipolar transistor is cutoff when there is no collector to emitter is effectively an open circuit. In digital application transistor in cut off mode is considered as OFF.

Saturation mode:

The operating mode of a bipolar transistor, when there is an increase in base current, will not cause a further increase in the collector current and path from collector to emitter is very nearly a short circuit. This is the ON state of a transistor in digital circuits.

It is modified circuit of DTL gate circuit

1. Multiple emitter of transistor T1 are connected to inputs, it behaves like the input diodes in DTL gate (common base). The base collector junction of T1 acts as another PN junction diode D4 in DTL gate.
2. Transistor T2 replaces the diode D5 in DTL gate. The output of TTL gate is taken from the open collector of T3.
3. R_L connected externally to IC package to pull-up the output to high voltage level, when T3 is OFF, else T3 acts as open circuit and a small amount of noise can change this to low level.
4. When T3 conducts, its collector will have a current path supplied by the input of the loading gate through V_{CC}, THE R1 resistor and forward biased base-emitter junction.

Low level voltage: 0.2V

High level voltage: 2.4 to 5V

Case i:

If any one of the inputs given to emitter of the transistor T1 is low, T1 conducts and it is turned ON giving minimum collector voltage. This minimum collector voltage is given to the base of the transistor T2 and it is turned OFF which acts as open circuit. Since emitter voltage of T2 is minimum and it is connected to the base of T3. T3 does not receive enough voltage to conduct therefore T3 is also turned OFF giving maximum collector voltage.

Output Y= HIGH, if any one input is low.

Case ii:

If all inputs given to the emitter of transistor T1 are high, then T1 does not conduct and is turned OFF acts as open circuit. Therefore the collector voltage of T1 is maximum. This maximum voltage is given to the base of T2 and thus T2 conducts and transistor T2 is turned ON. T2 giving a maximum emitter voltage and thus transistor T3 is also turned ON, gives a minimum collector voltage.

Output Y= LOW, if all the input are high.

Advantage:

1. More than one open collector output can connect to a single line. If all outputs attached to the line are in high-impedance state, the pull up resistor will hold the wire in high voltage (logic 1). If one or more device outputs are in ground (logic0) state, they will sink current and pull the

line voltage towards ground. This wired logic connection has several uses.

2. Open collector devices are commonly used to connect multiple devices to a bus. One carrying interrupt or write enable signals. If open collector devices are not used then the outputs of the inactive would attempt to hold the bus voltage high resulting in unpredictable output.

Limitations:

1. It is power consuming, since they tend to require higher current minimizes for correct operation.
2. Has high static power as there is always a direct current path from V_{CC} to ground and when the device is switched ON.
3. When it is in 'OFF' state they often have a few nanoamperes of leakage current.
4. The pull-up resistor is used at the output transistor which prevents the rapid charging of any wiring capacitance on the output. One way to improve the rise time is to reduce the resistance value but this increases the power dissipation when the output is low.

2)Totem-Pole Output of TTL circuit (NAND)

The addition of push-pull circuit in the output of the gate is called totem pole. If the output devices are driven by two or more signals of differing phase, the design is push-pull because of low output impedance. In open collector circuit, problem arises when the output is high and the pull-up resistor is too large. Ideally we would like to have a very low resistance pull-up when the output is high, but a very high pull-up resistance when the output is low. In this way, we could get quick charging and very low power dissipation. Totem pole TTL circuit has effective low impedances during '0' to '1' transition provides us an ability to connect its output to a capacitor.

Normally an output impedance of gate is resistive + capacitive load.

Capacitive load consist of capacitance of output transistor, capacitance of fan-out gates and any stray wiring capacitance.

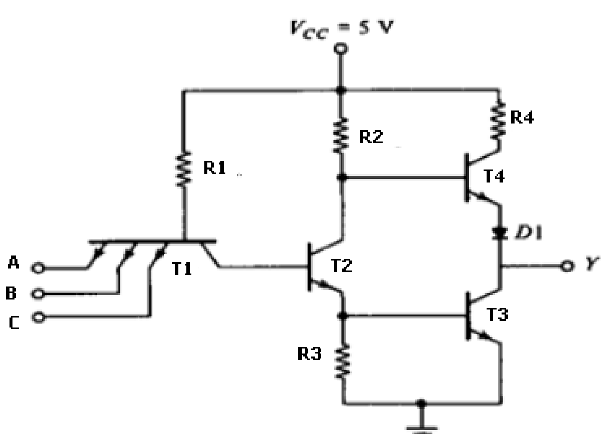


Table. Truth table for NAND

INPUTS			OUTPUT
A	B	C	Y
0	0	0	1
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Fig. Totem-Pole Output of TTL circuit (NAND logic)

When output of the transistor changes from low or high state when it goes from saturation to cut off, then the total capacitance 'C' charges exponentially from low to high voltage level with a time constant equal to RC.

In totem-pole the active pull-up resistor R_L in open collector is replaced by transistor T4 and diode D1.

1. When the output Y is in low state, T2 and T3 are driven into saturation as in open-collector gate. The voltage in collector of T2 is V_{BE}(T3)+V_{CE}(T2)=0.7+0.2=0.9V. The Output Y= V_{CE}(T2)=0.2V.
2. Transistor T4 is cutoff because its base must be one V_{BE} drop + one diode drop (or) 2x0.6=1.2V to start conducting.
3. Since the collector of T2 is connected to the base of T4, the later voltage is 0.9V instead of 1.2V, So T4 is cutoff.
4. The reason for placing the diode in the circuit is to provide a diode drop in the output path and thus ensure that T4 is cutoff when T3 is saturated.

Case i:

If any one of the input given to the emitter of transistor T1 is low, then the transistor T1 is turned ON, giving a minimum collector voltage which is given to base of transistor T2. Since T2 receives minimum voltage in base T2 it is turned OFF and acts as open circuit, giving a maximum collector voltage and minimum emitter voltage. The maximum collector voltage is given to the transistor T4, therefore it is turned ON, and giving maximum emitter voltage makes the diode D1 to conduct. Since emitter voltage of T2 is minimum, T3 is OFF results in maximum collector output.

Output Y= HIGH, If any one of the input is low

Case ii:

If all the inputs to the emitter of T1 is high then the transistor T1 is turned OFF, gives a maximum collector voltage and is connected to the base of T2.the maximum voltage in base of transistor T2 turns it ON, and the collector voltage is minimum and emitter voltage is maximum. T4 is OFF and diode D1 does not conduct, acts as open circuit. The maximum emitter in T2 is given to the base of T3 and it is turned ON, gives a minimum collector voltage.

Output Y=LOW, if all the inputs are high

Since current is needed to charge the load capacitance causes T4 to saturate momentarily, and the output voltage rises with a time constant RC. Transition from low to high level is much faster.

Advantages:

It has a Low output resistance at output logic '1'. The resistance R4 does not allow to increase the output resistance and its influence is compensated by the negative feedback.

Limitations:

It has decreased voltage level i.e., not more than 3.5V of the output logic'1', even if the output is unloaded.

3)Three state gate

Tri state or three state logic allows an output port to assume a high impedance state along with the logic '1' and logic'0' levels, which allows multiple circuits to share the output line. Example: data bus drivers.

Tri state buffer:

Tri-state buffer requires two inputs one is the data input and the other is enable or control input. A three state buffer input is controlled by output that can be turned "ON" or "OFF" by means of an external "control" or enable signal input. This control input can be either logic'0' or logic'1'.

Table. tri state buffer

Control input c	Input A	Output Y
0	0	High impedance
	1	
1	0	A
	1	

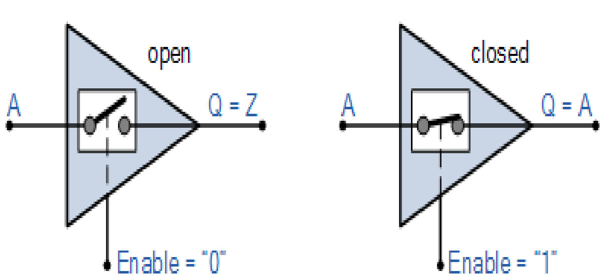


Fig. Tri state buffer logic

1. If the Control input C is high switch is closed the gate is enabled and the output is same as the input thus behaves like a normal buffer.

2. If the Control input C is low, the switch is open and instead of 'high' or 'low' outputs this gives a very high impedance (z) state, in which the buffer output is electrically disconnected from all the circuits and no current is drawn from the supply. then output is open circuit, gives high impedance.

Tristate buffer control:

A tri sate buffer is used as internal and external buses in microprocessor, computer memory and peripherals, I/O ,CPU, same data bus is carrying data with peripherals, I/O or memory it creates contention. Contention occurs when multiple devices are connected together, when in need to drive the device output to high or low.

The digital information is sent over these data highways either serially one bit at a time or it may be up to eight or more wires together in parallel form such as in microprocessor data bus allowing multiple tri-state buffer to be connected to the same data highway without damage or loss of data.

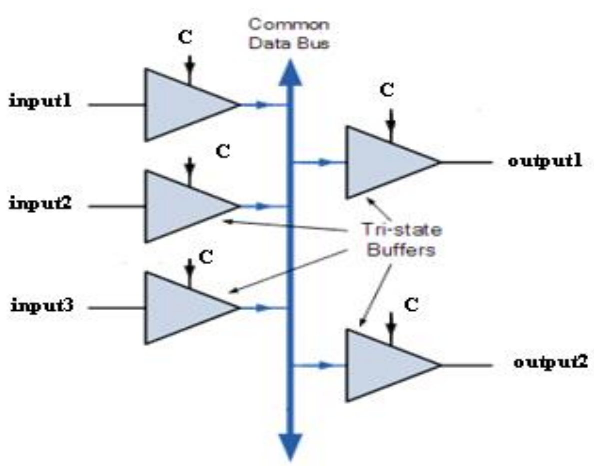


Fig. Data bus control with tri-state buffer

The tri-state buffer can be used to isolate devices from data bus and one another. Tri state buffers are connected together with decoders which are used to allow only one set of tri state buffer to be active at any one time making all other tri state buffers in high impedance

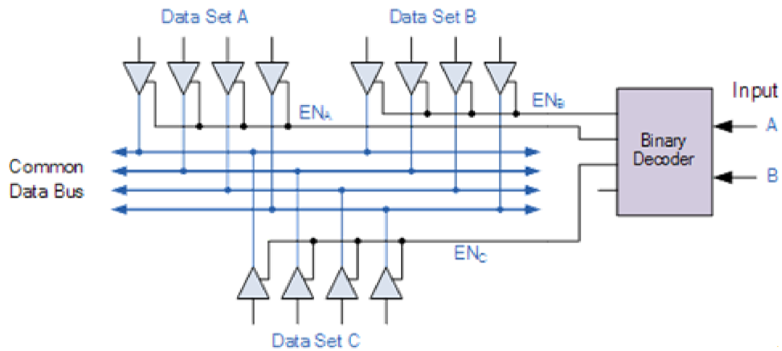
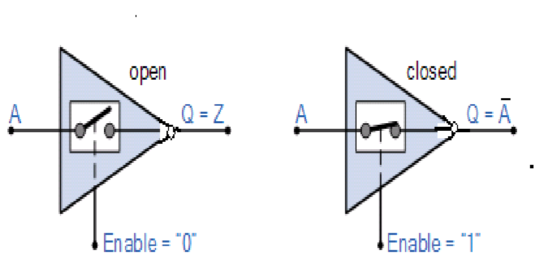


Fig. Tri state buffer control decoder

Tri state inverter

It requires two inputs one is the data input and the other is enable or control input. A three state inverter input is controlled by output that can be turned “ON” or “OFF” by means of an external “control” or enable signal input. This control input can be either logic’0’ or logic’1’.

Table. Tri-state inverter



Control input (C)	Input (A)	Output (Y)
1	0	$\bar{A}$ (complement of the input)
	1	
0	0	High impedance
	1	

Fig. Tri-state inverter logic diagram

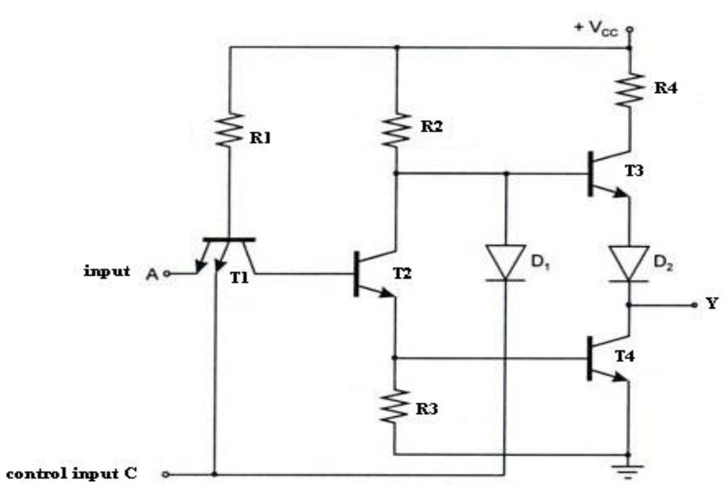


Fig. Tri-state inverter circuit

Case i:

If control input is low (for any data input A either '0' or '1') given to the emitter of transistor T1 is turned ON, giving a minimum collector voltage, this is given to the base of transistor T2. Since T2 receives minimum voltage is given to the base of T2 and it is turned OFF. This gives maximum collector voltage and minimum emitter voltage. The minimum emitter voltage of T2 is given to the base of T4, hence T4 is turned OFF.

The maximum collector voltage is bypassed through diode D1 since diode D1 conducts. Therefore T3 does not receive sufficient voltage hence T3 is turned OFF. Since both T3 and T4 are turned OFF, output is open circuited. This state is called high impedance state.

Output Y= High impedance state, if C is low for any input A.

Case ii:

a. If control input is high, and data input is low given to the emitter of transistor T1 hence it is turned ON. This gives a minimum collector voltage and maximum emitter voltage. The minimum collector voltage given to the base of transistor T2 turns it OFF, which gives maximum collector voltage and minimum emitter voltage.

   The maximum collector voltage from T2 is given to the base of T3 since D1 is reverse biased and does not conduct (open circuit) and makes the transistor T3 to turn ON (maximum emitter voltage).

   The minimum emitter voltage given to base of T4 and it is turned OFF (open circuit).

   Therefore output Y= HIGH, if input A is low.

b. If both control input and data input is high, given to the emitter of transistor T1 hence it is turned OFF. This gives a maximum collector voltage and minimum emitter voltage. The maximum collector voltage given to the base of transistor T2 turns it ON, which gives minimum collector voltage and maximum emitter voltage.

   The minimum collector voltage from T2 is given to the base of T3, since D1 is reverse biased and does not conduct (open circuit) and makes the transistor T3 to turn OFF.

The maximum emitter voltage given to base of T4 and it is turned ON.

Therefore output Y=LOW, if input A is high.

TTL logic uses a multi emitter transistor, a transistor with many emitter terminals. As every emitter is nothing but a diode, this logic eliminates these of all diodes. This is the major advantage. As transistor becomes ON and OFF much rapidly than a diode, switching time will be faster. TTL, or transistor-transistor logic replaced resistor-transistor logic, and used much less power. The TTL family is very fast and reliable, and newer faster, less power-consuming, etc.

4) SCHOTTKY TTL GATE:

A Schottky PN junction is made up of a semiconductor and a metal. This kind of junction has two characteristics: low turn-on voltage and low junction capacitance.

1. The turn-on voltage for the BC junction is lower, thus VCEsat is higher.
2. Due to lower junction capacitance, the transistor cannot go so deep into saturation.

Therefore Schottky TTL is thus faster than standard TTL and the terminal voltages are slightly different.

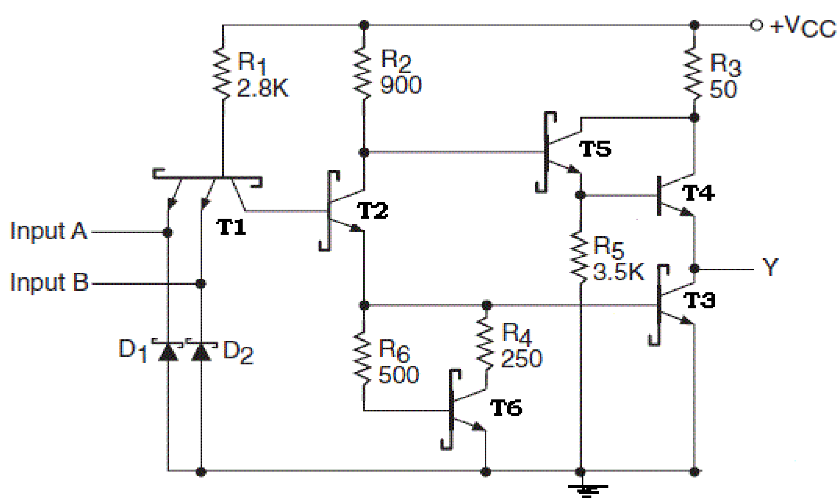


Fig. Schottky TTL circuit

Saturation delays the switching transistor from ON to OFF condition saturation can be eliminated by Schottky diode between base and collector prevents transistor going into saturation. The voltage across conducting Schottky diode is only 0.4V compared with 0.7V in conventional diode. The resulting transistor is called Schottky transistor except T4 , since it does not saturate but stays in active region.

Resistor values are reduced to decrease propagation delay further two new transistor T5 and T6 have been added Schottky diode are inserted between each input terminal and ground. T5 and T4 gives two V_{BE} drop to prevent T4 from conducting when output is low. This combination constitutes a double emitter-follower called Darlington pair.

It provides very high current gain and extremely low resistance exactly what is needed during low to high swing of output, resulting in decrease in propagation delay.

V)<u>EMITTER COUPLED LOGIC(ECL)</u>

Emitter coupled logic(ECL) is a high speed integrated circuit, ECL was invented in august 1956 at IBM by Hannon S.Yourke called as current steering logic. It uses a differential amplifier with single-ended input and limited emitter current to avoid saturated region of operation and its slow turn-off behavior. since the current is steered between two legs of an emitter coupled pair, it is called as current steering and this logic is also called as current mode circuits.

In this the transistors never go to saturation and the input/output voltages have a small swing(0.8V) the input impedance is high and the output resistance is low, therefore the transistors change states quickly. It has low gate delay and high fan-out.

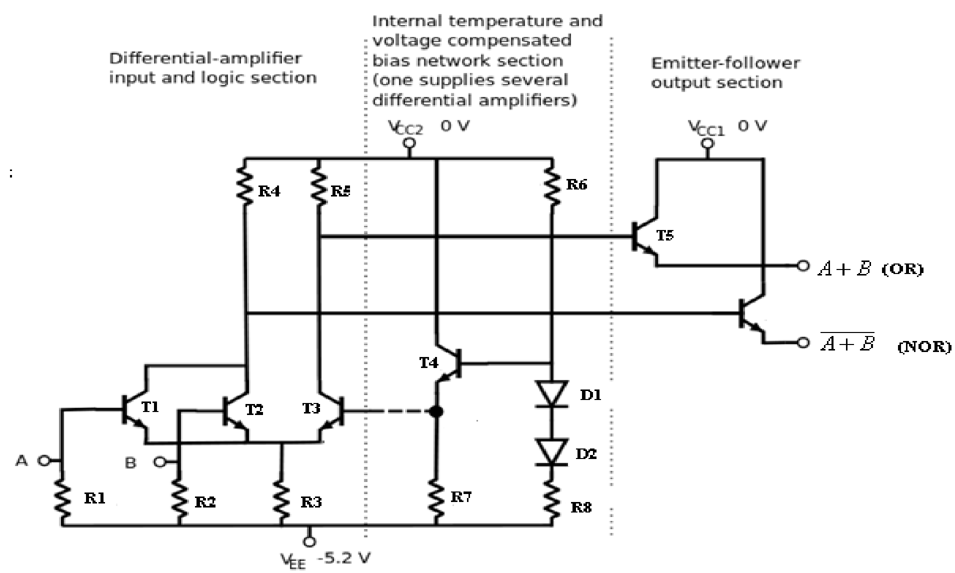


Fig. Two input ECL logic circuit

Table. Truth table for OR

INPUTS		OUTPUT
A	B	Y
0	0	0
0	1	1
1	0	1
1	1	1

Table. Truth table for NOR

INPUTS		OUTPUT
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

ECL circuit consist of differential amplifier input stage to perform logic, followed by an emitter follower to drive outputs and shift the output voltages. V_{CC} is connected to ground and V_{EE} is connected to -5.2V.

Positive logic: high= -0.9 V

Low= -1.7 V

Case i:

If both the inputs are low, transistor T1 and T2 is turned OFF, both emitter voltage is minimum and collector voltage is maximum. The minimum emitter voltage from T1 and T2 is given to the emitter terminal of T3, which turns ON. The maximum collector voltage from T1 and T2 is given to base of T6. Hence T6 is turned ON, gives HIGH emitter voltage. Therefore NOR output is HIGH. The minimum collector voltage from T3 is given to base of T5. Hence T5 is turned OFF, gives LOW emitter voltage. Therefore OR output is LOW.

Case ii:

If both the inputs are high, transistor T1 and T2 is turned ON, both emitter voltage is maximum and collector voltage is minimum. The maximum emitter voltage from T1 and T2 is given to the emitter terminal of T3, which turns OFF. The minimum collector voltage from T1 and T2 is given to base of T6. Hence T6 is turned OFF, gives LOW emitter voltage. Therefore NOR output is LOW. The maximum collector voltage from T3 is given to base of T5. Hence T5 is turned ON, gives HIGH emitter voltage. Therefore OR output is HIGH.

Case iii:

If any one of the inputs is high (A=0 and B=1), transistor T1 is turned OFF and T2 is turned ON. T2 emitter voltage is maximum which is given to the T3 emitter, makes it OFF produces a maximum collector voltage which is given to the base of T5. The transistor T5 is turned ON therefore gives a maximum emitter voltage. Hence OR output is HIGH. Since T1 is turned OFF and becomes open and T2 is ON the minimum collector voltage is given to T6 making the transistor OFF. Therefore emitter voltage is minimum and NOR output is LOW.

Case iv:

If any one of the inputs is high (A=1 and B=0), transistor T1 is turned ON and T2 is turned OFF. T1 emitter voltage is maximum which is given to the T3 emitter, makes it OFF produces a maximum collector voltage which is given to the base of T5. The transistor T5 is turned ON therefore gives a maximum emitter voltage. Hence OR output is HIGH. Since T2 is turned OFF and becomes open and T1 is ON the minimum collector voltage that is given to T6 making the transistor OFF. Therefore emitter voltage is minimum and NOR output is LOW.

Since ECL transistors do not saturate, it is possible to achieve propagation delays as low as 1-2 ns. This ECL logic family has lowest propagation delay of any family and is used mostly in system requiring very high speed operation. Its noise immunity and power dissipation however are worst of all logic families available.

Advantages:

1. Since no saturation of transistors small logic voltage swings (0.8V or less) therefore fastest switching speed circuits.
2. Due to the large output current propagation time is from 0.2 to 1ns.
3. Constant current from supply setting V_{CC} to 0V eliminates ripple.
4. Has high power dissipation.

Limitations:

1. More power consuming circuit, Since it consumes more power it is used only when high speed is required.
2. Each gate continuously draws current, which means it requires significantly more power than those of other families.
3. More different power supply voltages are needed and both PNP and NPN transistors are required.

VI) METAL OXIDE SEMICONDUCTOR

MOS devices can be used as transistor and also as resistors. A resistor is obtained from MOS by permanently biasing the gate terminal for conduction. The value of resistance is determined by the ratio of source to drain voltage to the channel.

(a) p-channel (b) n-channel

Fig. Symbol of MOS transistors

p-channel: gate logic 0-ON state, logic 1-OFF state

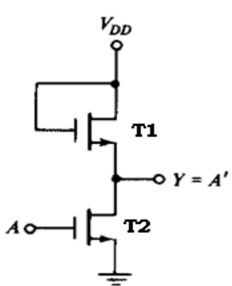
n-channel: gate logic 1-ON state, logic 0-OFF state

for an n-channel MOS the supply voltage V_{DD} is positive (about 5V) to allow positive current flow from drain to source. the two voltage levels are a function of threshold voltage V_T . The low voltage level is anywhere from 0 to V_T and high level ranges from V_T to $V_{DD.}$ n-channel gate usually positive logic. the p-channel MOS circuits use a negative voltage for inverter $V_{DD,}$ to allow positive current flow from source to drain.the two voltage levels are both negative above and below the negative threshold voltage V_T.p-channel gate employ negative logic.

1 NMOS Inverter Logic

T1 acts as load resistor and T2 as a active device. The load resistor MOS has its gate connected to V_{DD}, thus maintaining it in the conduction sate.

Table. Truth table of NOT



Input	Output
1	0
0	1

Fig. NMOS inverter logic

NMOS transistor T1 gate terminal is always connected with V_{DD}, thus T1 will be always ON.

Case i:

If the low input is given to the gate of the transistor T2, it turns OFF and acts as open circuit. Therefore V_{DD} passes through transistor T1 and gives a high output.

Output Y=High

Case ii:

If high input is given to the gate of the transistor T2, which turns ON and acts short circuit. Therefore output is ground.

Output Y=Low

NMOS NAND logic

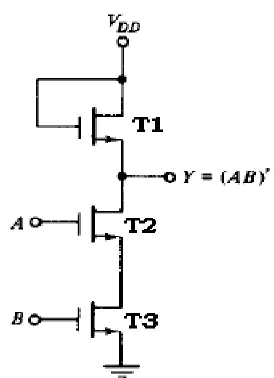
NMOS transistor T1 gate terminal is always connected with V_{DD}, thus T1 will be always ON.

Case i:

If both the inputs are low then T2 and T3 turns OFF, which acts as open circuit. Therefore V_{DD} passes through transistor T1and gives an high output.

Output Y=high

Table. Truth table of NAND



INPUTS		OUTPUT
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Fig. NMOS NAND logic

Case ii:

If both the inputs to the gate of NMOS T2 and T3 are high, both the transistor are turned ON. T1, T2, T3 are all short circuited, therefore the circuit gives a low output.

Output Y=Low

Case iii:

If any of the input is low (A=0 and B=1 (or) A=1 and B=0) the corresponding NMOS transistor which gets high input to the gate terminal will turn ON and the other is OFF. Therefore the circuit acts as open circuit, gives a high output.

Output Y=high

NMOS NOR logic

NMOS transistor T1 gate terminal is always connected with V_{DD}, thus T1 will be always ON.

Table. Truth table for NOR

INPUTS		OUTPUT
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

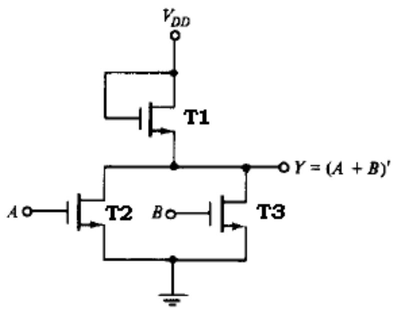


Fig. NMOS NOR logic

Case i:

If both the inputs are low then T2 and T3 turns OFF, which acts as open circuit. Therefore V_{DD} passes through transistor T1and gives an high output.

Output Y=high

Case ii:

If both the inputs to the gate of NMOS T2 and T3 are high, both the transistor are turned ON. T1, T2, T3 are all short circuited, therefore the circuit gives a low output.

Output Y=Low

Case iii:

If any of the input is low (A=0 and B=1 (or) A=1 and B=0) the corresponding NMOS transistor which gets high input to the gate terminal will turn ON and the other is OFF. Therefore the circuit acts as short circuit, gives a low output.

Output Y=low

Advantages:

1. Reduce the complexity of the circuit i.e., fabricate fast and low-cost with simple circuit.
2. Has low static power consumption
3. High noise immunity
4. high density of logic function on a chip

Limitation:

NMOS circuits are slow to transition from low to high. When transitioning from high to low, the transistors provide low resistance, and the capacitative charge at the output drains away very quickly (similar to discharging a capacitor through a very low resistor). But the resistance between the output and the positive supply is much greater, so the low to high transition takes longer (similar to charging a capacitor through a high value resistor). Using a resistor of lower value will speed up the process but also increases static power dissipation. However, a better (and the most common) way to make the gates faster is to use depletion-mode transistors instead of enhancement-mode transistors as loads. This is called depletion-load NMOS logic.

VII) COMPLEMENTARY MOS TRANSISTORS(CMOS)

TTL logic gate series are based on bipolar transistor logic technology and they are current operating devices, normally consumes large amount of power from at a fixed +5V power supply, this is one disadvantage.

Secondly, TTL gates have limited operating speed when switched from OFF to ON and Vice-versa, resulting in gate or propagation delay.

To overcome this we go to Complementary MOS logic gates using Field effect transistor. These gates have both P-channel and N-channel, with no switching. The power consumption of CMOS gates is almost zero, making them ideal for use in low power battery circuits and with switching speeds upwards of 100MHz for use in high frequency timing and computer circuits.

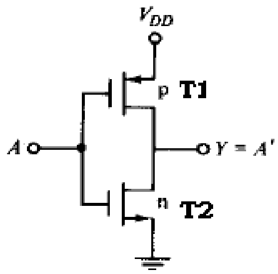
Both n-channel and p-channel device can be fabricated on the same substrate

1. n-channel MOS conducts when its gate-to-source voltage is positive.
2. p-channel MOS conducts when its gate-to-source voltage is negative.
3. Either type of device is turned OFF if its gate-to-source voltage is zero.

1)CMOS Inverter logic

The source terminal of p-channel device is at V_{DD} and the source terminal of n-channel device is at ground.

Table. Truth table of NOT



Input	Output
1	0
0	1

Fig. CMOS Inverter logic

Case i:

If Input to the transistor A is low then both gates are at zero potential. The input is at $-V_{DD}$ relative to source of p-channel and at 0V relative to source of n-channel. Therefore p channel is turned ON and n-channel is turned OFF, gives an high output.

Output Y is HIGH.

Case ii:

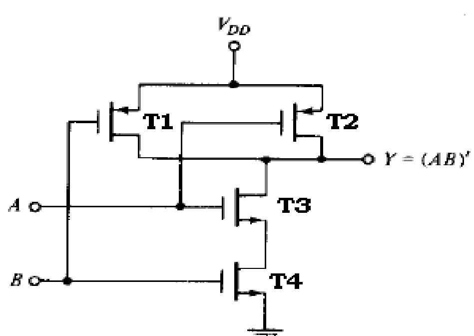
If the Input to the transistor A is high then both gate are at V_{DD} and is reversed. Therefore p channel is turned OFF and n-channel is turned ON, giving a low output.

Output Y is LOW.

2)CMOS NAND logic

The two input NAND gate consist of two p-type unit in parallel and two n-type unit series.

Table. Truth table of NAND



INPUTS		OUTPUT
A	B	Y
0	0	1
0	1	1
1	0	1
1	1	0

Fig. CMOS NAND logic

Case i:

If both the inputs are low then p-type T1 and T2 turns ON whereas n-type T3 and T4 turns OFF, which acts as open circuit. Therefore V_{DD} passes through transistor T1and T2, gives an high output.

Output Y=high

Case ii:

If both the inputs to the gate of p-type T1 and T2 are high, both the transistor are turned OFF whereas n-type T3and T4 turns ON therefore the circuit gives a low output.

Output Y=Low

Case iii:

If any of the input is low (A=0 and B=1) the corresponding p-type transistor T2 turns ON and T1 turns OFF, whereas n-type transistor T3 OFF and T4 turns ON. Therefore the circuit acts as open circuit, gives a high output.

Output Y=high

Case iv:

If any of the input is low (A=1 and B=0) the corresponding p-type transistor T2 turns OFF and T1 turns ON, whereas n-type transistor T3 ON and T4 turns OFF. Therefore the circuit acts as open circuit, gives a high output.

Output Y=high

3)CMOS NOR logic

Two input NOR gate consist of two n-type unit in parallel and two p-type its in series.

Fig. CMOS NOR logic

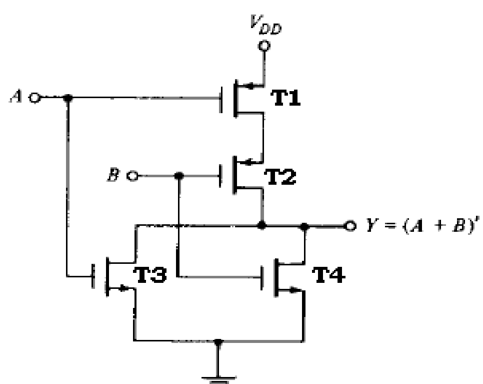


Table. Truth table of NOR

INPUTS		OUTPUT
A	B	Y
0	0	1
0	1	0
1	0	0
1	1	0

Case i:

If both the inputs are low then p-type T1 and T2 turns ON whereas n-type T3 and T4 turns OFF, which acts as open circuit. Therefore V_{DD} passes through transistor T1and T2, gives a high output.

Output Y=high

Case ii:

If both the inputs to the gate of p-type T1 and T2 are high, both the transistor are turned OFF, whereas n-type T3 and T4 turns ON. therefore the circuit gives a low output.

Output Y=Low

Case iii:

If any of the input is low (A=0 and B=1) the corresponding p-type transistor T2 turns OFF and T1 turns ON, whereas n-type transistor T3 OFF and T4 turns ON. Therefore the top circuit acts as open circuit, gives a low output.

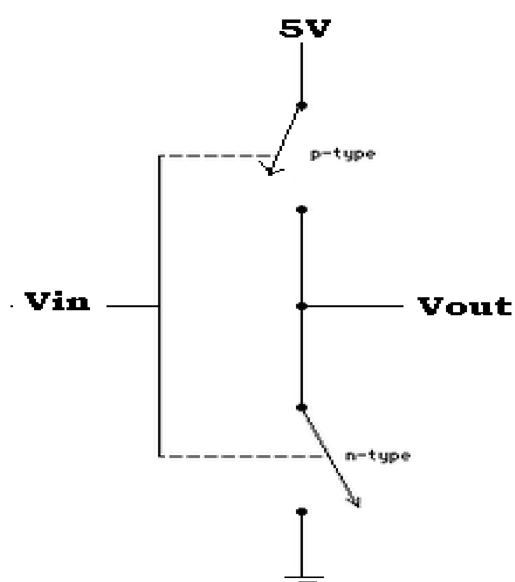
Output Y=low

Case iv:

If any of the input is low (A=1 and B=0) the corresponding p-type transistor T2 turns ON and T1 turns OFF, whereas n-type transistor T3 ON and T4 turns OFF. Therefore the top circuit acts as open circuit, gives a low output.

Output Y=low

4)CMOS inverter as two switches



V_{in} =Low voltage: upper switch (p) closes, therefore output is high voltage (V_{OUT})

V_{in} =high voltage: lower switch (n) closes. Therefore output is ground

V_{OUT}=complement of V_{in}

Here arrows to indicate channel type is omitted and gate input of p-channel is drawn with an inversion bubble enabled with low voltage

Input=low upper transistor conducts making logic 1

Input=high lower transistor conducts making logic 0

Therefore CMOS inverter

Advantages:

1. Both n-channel and p-channel devices can be fabricated together on the same substrate material.
2. Improves the switching speed and propagation delay.
3. Has less power consumption.
4. Very low static power consumption in compare with NMOS technology.

Limitations:

1. They can be easily damaged by static electricity. Therefore extra care has to be taken when handling the device.
2. It operates in single supply voltage of between +3 and +18 Volts. Lowering the supply voltage reduces the charge stored on any capacitances and consequently reduces the energy required for a logic transition. Reduced energy implies less heat dissipation. By lowering the power supply from 5V to 3.3V, switching power was reduced by almost 60 percent (power dissipation is proportional to the square of the supply voltage). Newer CPUs have lowered their power supply voltages further.
3. CMOS technology is more complex to fabricate than NMOS technology, so it is more expensive.

VIII)CMOS COMPARED TO TTL:

- CMOS components are typically more expensive than TTL equivalents. However, CMOS technology is usually less expensive on a system level due to CMOS chips being smaller and requiring less regulation.

- CMOS circuits do not draw as much power as TTL circuits while at rest. However, CMOS power consumption increases faster with higher clock speeds than TTL does. Lower current draw requires less power supply distribution, therefore causing a simpler and cheaper design.
- Due to longer rise and fall times, the transmission of digital signals becomes simpler and less expensive with CMOS chips.
- CMOS components are more susceptible to damage from electrostatic discharge than TTL components.

IX)CHARACTERISTICS OF LOGIC FAMILIES

Characteristics of RTL:

1. Operating speed is low, i.e., propagation delay of the order of 500ns, it cannot operate at speed above 4Mhz.
2. Poor noise immunity
3. Power dissipation is very high.
4. It is temperature sensitive circuits.
5. Fan out is 4 or 5 with a switching delay of 50ns and fan in is 4.

Charactersistics of DTL family:

1. The propagation delay of DTL is 25ns, in this the turn off delay is larger than turn on delay by a factor of 2 or 3.
2. It has high noise margin, due to additional diode D5 connected to D4. when the output is low the noise margin is 0.8 V and when the output is high, the noise margin is 3.4V.
3. Fan out is 8 which is higher than RTL.

Characteristics of TTL:

1. It has average power dissipation of about 10mW per gate.
2. Since the propagation delay is 10ns, the switching speed is fast.
3. Its fan out is 10 and drives 10 standard TTL inputs.
4. It has a fixed 5V power supply. Both 74 series and 54 series can operate at 5V.
5. It has greater tolerance to temperature and voltage.
   74 series works with 0 to 70^0C
   54 series works with -55^0 to $+125^0$C.
6. It has less noise immunity than CMOS.

Characteristics of ECL:

1. In this type the transistors are not allowed to go into complete saturation due to this the transistors are kept close to each other and thus eliminating storage delays and also consumes high power.

2. The logic level are kept close to each other to reduce noise margin and it is very difficult to achieve good noise immunity.
3. Since the power supply current are more stable than TTL and CMOS circuits power consumption is high.
4. This is the fastest if all the logic families, since its propagation delay is 500ps.

Characteristics of NMOS:

1. This has a propagation delay of 50ns.
2. Its noise margin is about 1V.
3. It can be easily operated at a fan out of 50.
4. It is fabricated by only one basic element which doesnot require any resistor, diode etc., and lower power dissipation make easy foe LSI.

Characteristics of CMOS:

1. Less power consuming.
2. It is called active power dissipation because the average power dissipation of CMOS devices whose output is continuously changing.
3. Propagation delay ranges from 25 to 150ns.
4. The noise margin is about 45% of the supply voltage V_{DD}.
5. it works over a temperature

    74 series works with -40^0 to $+85^0$C

    54 series works with -55^0 to $+125^0$C.